MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

Operating Manual

Programming unit
type A7PU

your s

MITSUBISHI ELECTRIC

-A

REVISIONS

※The manual number is given on the bottom left of the back cover.

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers.
Please read this manual carefully so that the equipment is used to its optimum.
A copy of this manual should be forwarded to the end User.

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1. GENERAL DESCRIPTION

The A7PU programming unit (hereinafter referred to as "PU") is a programming unit with audio cassette interface used for the MELSEC-A series.
This Operating Manual describes the operations of the PU.
This manual is structured as follows:

Differences between Type A6PU Programming Unit and Type A7PU Programming Unit are as described below:

1) ROM cassettes for A6PU and A7PU are not compatible with each other.
2) Applicable CPU types are as indicated in the following table. (○: Usable, X: Unusable)

CPU Type \ PU Type	A6PU	A7PU
A0J2CPU	X	○
A1CPU, A1ECPU, A1NCPU	○	○
A2CPU, A2ECPU, A2NCPU	○	○
A3CPU, A3ECPU, A3NCPU	○	○
A3HCPU	X	○

After unpacking, make sure that the package includes the following products.

Description	Quantity
Type A7PU programming unit	1
Type J-1 cable (for connection with audio cassette recorder)	1

POINT

In using the PU, refer to the following manuals as required:

- **A series CPU User's Manual.**
- **Instruction Manual for the audio cassette used.**

2. SYSTEM CONFIGURATION

This chapter describes system configurations with which the PU may be used.

2.1 Applicable System

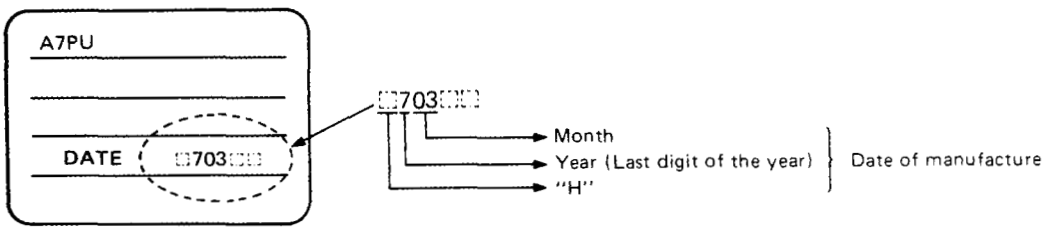
The PU has a programming function and an audio cassette function. If may be used in the following two ways in conjunction with the A series PC:

1) Add-on system: The PU is connected directly onto the A series CPU.

2) Hand-held system: The PU is connected to the A series CPU with the AC30R4 (AC300R4) cable (for A6GPP).

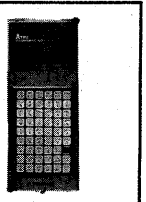
Example configurations are shown in Fig. 2.1 and Fig. 2.2 on the following pages.

A7PUs manufactured after March, 1987 or those which have an H before the date of manufacture may be used with the A3HCPU (P21/R21). The name plate shown below indicates the date of manufacture.

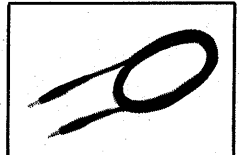


(1) Add-on system

Type	Building block type CPU



Type	A7PU



Type	J-1 (cable)

Audio cassette

Fig. 2.1 System Configuration Example

(2) Hand-held system

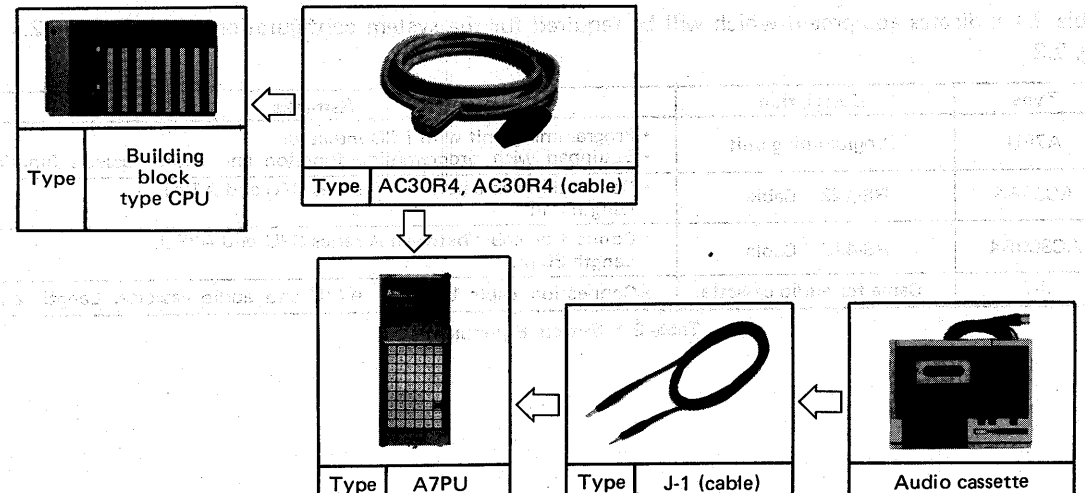


Fig. 2.2 System Configuration Example

2.2 System Equipment

Table 2.1 indicates equipment which will be required for the system configurations shown in Fig. 2.1 and Fig. 2.2.

Type	Description	Remarks
A7PU	Programming unit	• Programming unit with LCD indicator • Equipped with programming function and audio cassette function
AC30R4	RS-422 Cable	• Connection cable between A series CPU and A7PU. Length 3 m.
AC300R4	RS-422 Cable	• Connection cable between A series CPU and A7PU. Length 30 m.
J-1	Cable for audio cassette	• Connection cable between A7PU and audio cassette. Length 2 m.

Table 2.1 System Equipment List

3. SPECIFICATIONS

Describes the performance specifications of the PU.

3.1 General Specifications

The general specifications of the PU are as indicated below:

Item	Specifications					
Ambient temperature	Operating	0 to 40°C				
	Storage	−20 to 50°C				
Ambient humidity	Operating	85%RH or less (no condensation)				
	Storage	10 to 90%RH or less (no condensation)				
Vibration resistance	Conforms to JIS C9011.		Frequency	Acceleration	Amplitude	Sweep count
			10 to 55Hz	—	0.075mm	10 times
			55 to 150Hz	1g	—	(1 octave/minute)
Shock resistance	Conforms to JIS C0912. (10g, 3 times in each of X, Y, and Z directions)					

Table 3.1 General Specifications of A7PU (Continue)

Item	Specifications
Operating ambience	There should be no corrosive gases and dust should be minimum.
Cooling system	Self-cooling

Table 3.1 General Specifications of A7PU

3.2 A6PU Performance Specifications

The performance specifications of the PU are as indicated below:

Item	Specifications	
Connected unit	A series PC	
Power, current consumption	Power supplied from connected A CPU (5V DC, 0.3A)	
Connection system	Add-on	Loaded to A series CPU directly.
	Hand-held	Connected by AC30R4 cable.
Display system	Display of 16 characters x 2 lines (with cursor) (liquid crystal display) Equipped with illumination for the display	
Operation system	54 operation keys (Covered by polyurethane film)	
Key operation check	Buzzer	
Audio cassette interface	Applicable audio cassette	Domestic audio cassette recorder (See Appendix 1).
	Applicable tape	Any domestic cassette tape (particularly home computer types)
	Transmission speed	600 BPS
	Record output/replay output	100mVp-p/5Vp-p

Table 3.2 Performance Specifications of A7PU (Continue)

Item	Specifications
External dimensions mm (inch)	188 (7.40) (height) x 79 (3.11) (width) x 44.5 (1.75) (depth). When loaded directly to CPU, depth is 37.5 (1.48).
Weight kg (lb)	0.5 (1.1)

Table 3.2 Performance Specifications of A7PU

3.3 Connection Cables

The specifications of connection cables required for the PU are as indicated below.

(1) AC30R4 cable

Item	Specifications
Connected CPU	Between A series CPU and A7PU
Length m (ft)	3 (9.84)
Weight kg (lb)	0.5 (1.1)

Table 3.3 AC30R4 Cable

(2) AC300R4 cable

Item	Specifications
Connected CPU	Between A series CPU and A7PU
Length m (ft)	30 (98.4)
Weight kg (lb)	5 (11)

Table 3.4 AC300R4 Cable

(3) J-1 cable

Item	Specifications
Connected unit	Between A7PU and audio cassette recorder
Length m (ft)	2 (6.56)
Weight kg (lb)	0.03 (0.07)

Table 3.5 J-1 Cable

4. HANDLING

This chapter describes the handling instructions, nomenclature, and maintenance of the PU.

4.1 Handling Instructions

(1) Do not drop or subject to shock.

(2) Do not disassemble the case.

(3) When the PU is not in use or the PU is connected to the CPU via a cable, fit the protective cap on to the connector.

(4) Do not touch the connector pins of the PU.

(5) Do not open the ROM cartridge container and do not remove the ROM cartridge located inside.

IMPORTANT

(1) When designing the system, ensure that all protective and safety circuits are located outside the PC.

(2) Static electricity will damage the components on the printed circuit board therefore:

1) Ground human body and work bench.
2) Do not touch the conductive areas of the printed circuit board or the components with any non-grounded material.

4.2 Nomenclature

The nomenclature of the PU is indicated in Fig. 4.1 and Fig. 4.2.

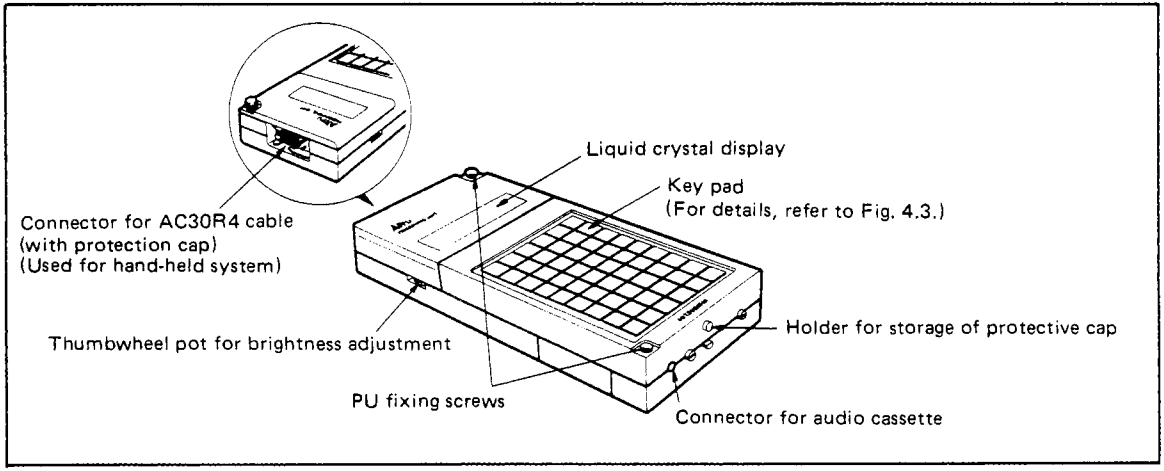

Liquid crystal display
Key pad
(For details, refer to Fig. 4.3.)
Connector for AC30R4 cable
(with protection cap)
(Used for hand-held system)
Thumbwheel pot for brightness adjustment
Holder for storage of protective cap
PU fixing screws
Connector for audio cassette

Fig. 4.1 Nomenclature of A7PU (front)

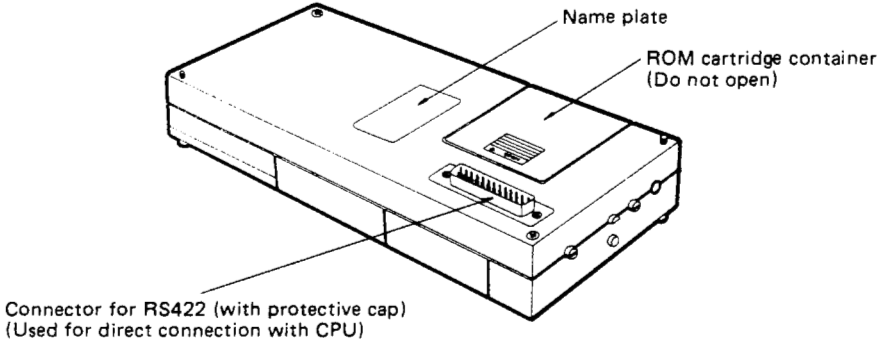

Name plate
ROM cartridge container
(Do not open)
Connector for RS422 (with protective cap)
(Used for direct connection with CPU)

Fig. 4.2 Nomenclature of A7PU (rear)

The arrangement of operation keyboard is shown in Fig. 4.3.

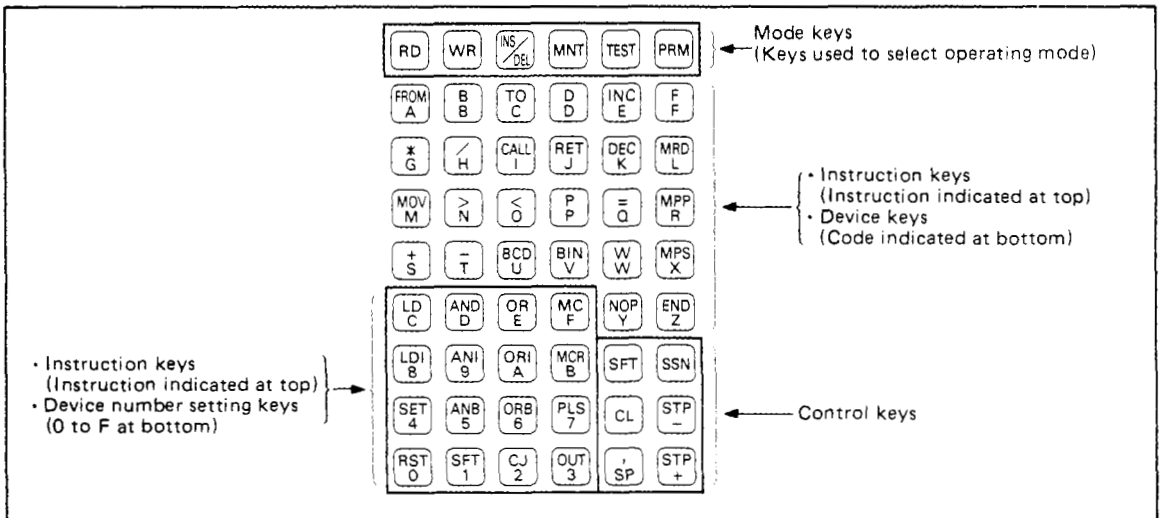


Fig. 4.3 Arrangement of Operation Keyboard

4.3 Maintenance

The PU has no special components which require inspection or replacement.

When keeping the PU in storage, take care of the following points:

(1) Avoid storing the PU in the following environments:

1) Ambient temperature is outside the range −10°C to 50°C.
2) Ambient humidity is outside the range 10 to 90%RH.
3) Condensation occurs due to sudden temperature changes.
4) Anywhere that the PU may be subjected to wind and rain or the direct rays of the sun.
5) Anywhere that there are excessive amounts of conductive powders, such as dust, dirt, and iron filings, or corrosive gases, oil mist, salt, etc.

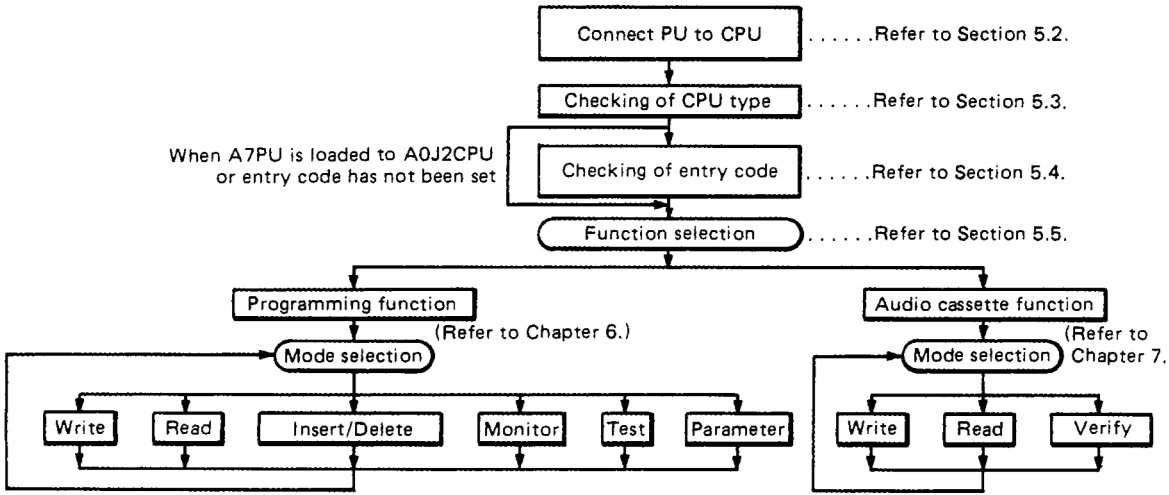
(2) Ensure that the audio cassette manual is fully understood before use.

(3) Avoid storing tape cassettes in places where temperature and/or humidity are high or in the vicinity of strong magnetic fields.

(4) When storing a cassette for a long time, replay and rewind it on the cassette player every six months.

5. STARTING PROCEDURE

5.1 Starting Procedure and General Operation Procedure



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5.2 Connecting and Disconnecting to and from the A Series CPU

The PU can be connected and disconnected to and from the PC while it is running. If possible, however, connect and disconnect the PU with the PC in STOP mode. When connecting and disconnecting the PU with the PC in RUN mode take care to insert the connector properly.

Fig. 5.1 shows the connecting and disconnecting procedures for direct connection with the PC and Fig. 5.2 shows the connecting and disconnecting procedures for remote connection.

When using the audio cassette function, connect the PU according to Fig. 5.1 or Fig. 5.2, and then connect the PU and the audio cassette according to Fig. 5.4.

(1) Connecting procedure
   1) Remove the CPU connector cap.
   2) Remove the RS422 connector protective cap at the rear of the PU. Store the protective cap by clipping it to the lugs on the bottom of the PU. (Refer to Fig. 5.5.)
   3) As shown at left, connect the PU and the PC.
   4) Tighten the PU fixing screws.

(2) Operation
   Perform operation according to Chapter 6 or Chapter 7.

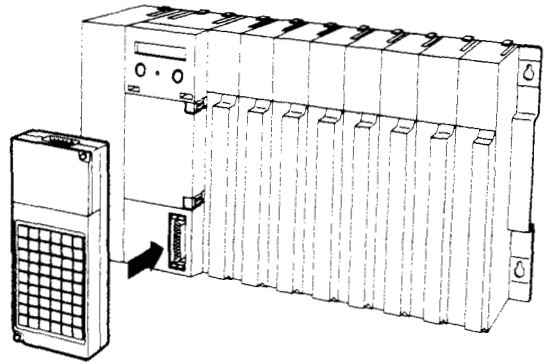


Fig. 5.1 Connection and Disconnection Procedures for direct connection with CPU.

(3) Disconnecting procedure

1) Press the CL key.
2) Remove the PU fixing screws.
3) Unload the PU from the CPU.
4) Fit the RS422 connector protective cap to the rear of the PU.
5) Fit the CPU connector cap.

(1) Connecting procedure

1) Remove the CPU connector cap.
2) Remove the protective cap from the connector at the top of the PU. Store the protective cap by clipping it to the lugs on the bottom of the PU. (Refer to Fig. 5.5.)
3) Connect the plastic cased connector on the AC30R4 to the socket on the top of the PU.
4) Connect the metal cased connector to the RS422 socket on the CPU and tighten the fixing screws.

(2) Operation

Perform operation according to Chapter 6 or Chapter 7.

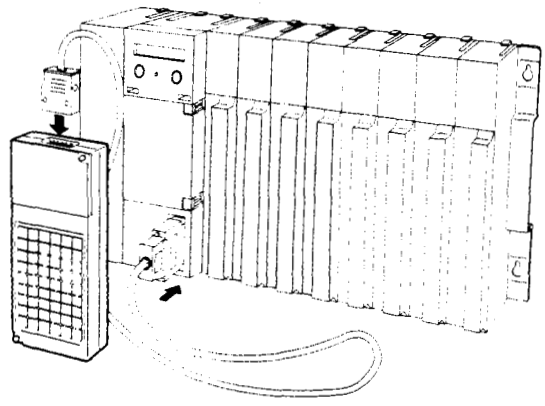
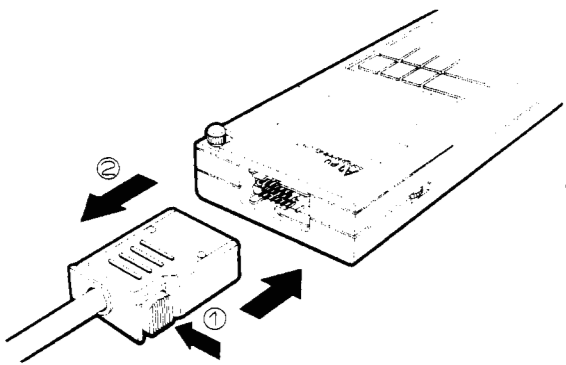


Fig. 5.2 Connecting and Disconnecting Procedures for Remote Connection with CPU

(3) Unloading procedure

1) Press the CL key.
2) Remove the fixing screws on the CPU connector and disconnect the AC30R4 cable from the CPU. Fit the cap to the CPU connector.
3) Disconnect the AC30R4 cable from the PU.
4) Fit the protection cap to the connector on the top of the PU.

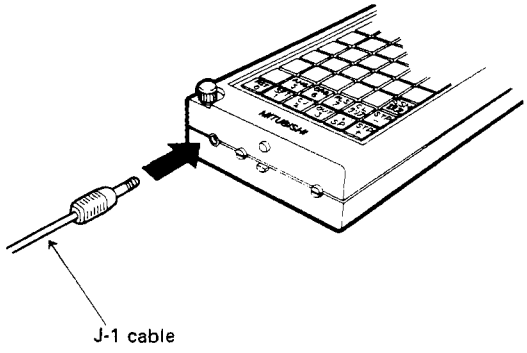
For connecting ans disconnecting of the AC30R4 cable to and from the connector at the top of the PU, refer to Fig. 5.3.



(1) Connection of PU and AC30R4 cable
Insert the PU connector end of the AC30R4 cable into the PU in the direction shown on the left. (Insert the connector until clicking sound is heard.)

(2) Disconnection of PU and AC30R4 cable
1) Push the connector release button in the direction of arrow ①.
2) With the button pressed, pull the connector in the direction of arrow ②.

Fig. 5.3 Connecting and Disconnecting of PU and AC30R4 Cable



(1) J-1 to PU

As shown on the left, connect the cable to the audio cassette connector at the bottom of the PU.

(2) Connection to audio cassette

○ Write mode

Connect the cable to the microphone terminal or equivalent of audio cassette recorder.

○ Read and verify modes

Connect the cable to the earphone terminal or equivalent of audio cassette recorder.

Fig. 5.4 Connection with Audio Cassette

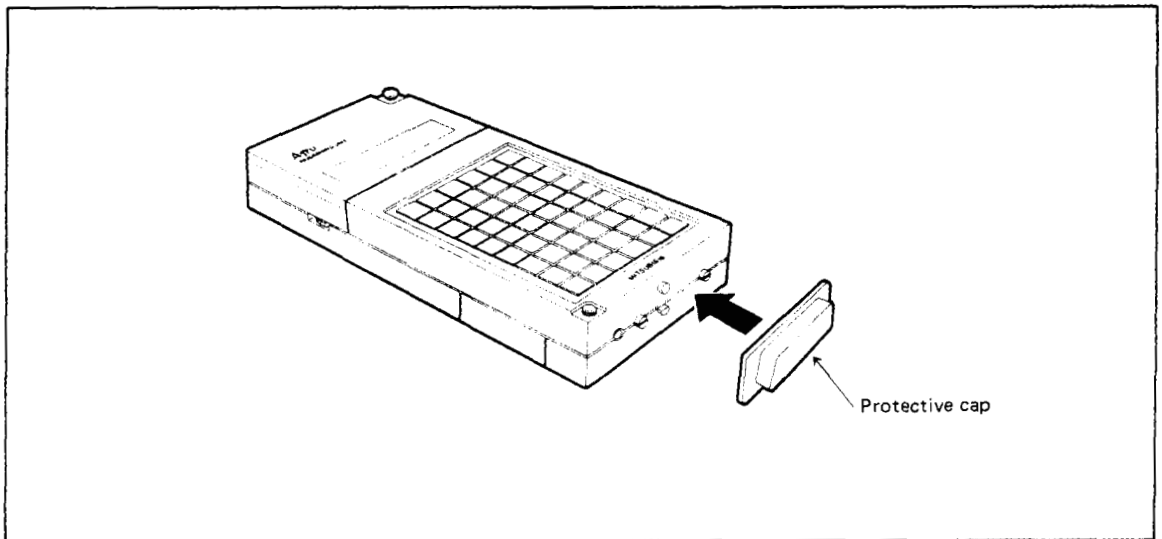


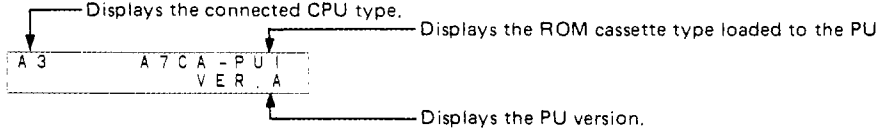
Fig. 5.5 Storing of protective cap

5.3 Checking of CPU Type

Basic Operation [STP ±]

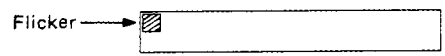
(1) By the input of [STP ±]
When an entry code has been specified, proceed to Section 5.4.
When the A7PU is loaded into the A0J2CPU or an entry code has not been specified, proceed to Section 5.5.

(2) When the PU is connected with the CPU or the PU is reset (refer to Section 5.6), the following screen is displayed.



REMARKS

After the PU is connected to the CPU, it takes 3 to 5 seconds until the screen shown on the left is displayed. Before this screen is displayed, the status of screen is as shown below. (The same applies during communication with the ACPU.)



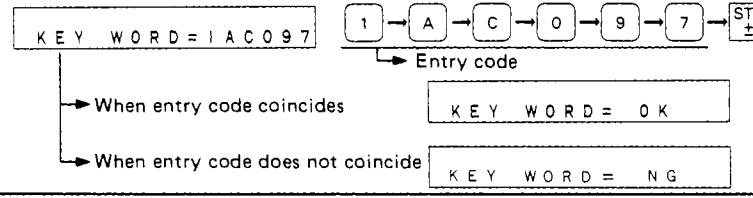
5.4 Checking of Keyword (or Entry Code) (only applicable if an entry code has been entered into the parameters)

Basic Operation

[Entry code input operation] → [STP ±]

Only the device number setting keys (0 to F) may be pressed.

Operation Procedure

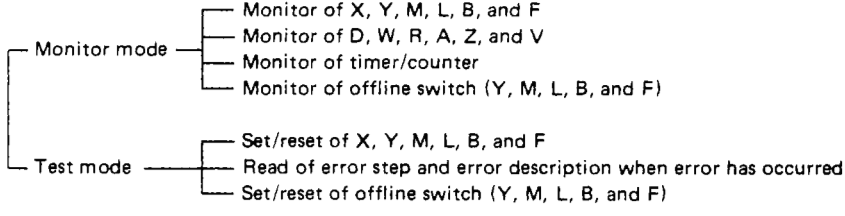


REMARKS

[STP ±] indicates that the [STP +] or [STP −] key is input.

When the CPU type checking operation is performed after the entry code is specified (6-digit hexadecimal number), the keyword input screen is displayed.
When a keyword has not been entered or A7PU is loaded in A0J2CPU, the screen shown in Section 5.5 is displayed.

1) Input the six digit hexadecimal data using the device number setting keys.
2) Check the keyword. After OK/NG has been displayed for two seconds, the screen shown in Section 5.5 is displayed. When keyword and entry codes do not coincide, only the following operations are valid.


Monitor mode
Monitor of X, Y, M, L, B, and F
Monitor of D, W, R, A, Z, and V
Monitor of timer/counter
Monitor of offline switch (Y, M, L, B, and F)
Test mode
Set/reset of X, Y, M, L, B, and F
Read of error step and error description when error has occurred
Set/reset of offline switch (Y, M, L, B, and F)

5.5 Function Selection

Basic Operation

(SFT) STP ±

Function selection

Operation Procedure

PROGRAMMING

STP ±

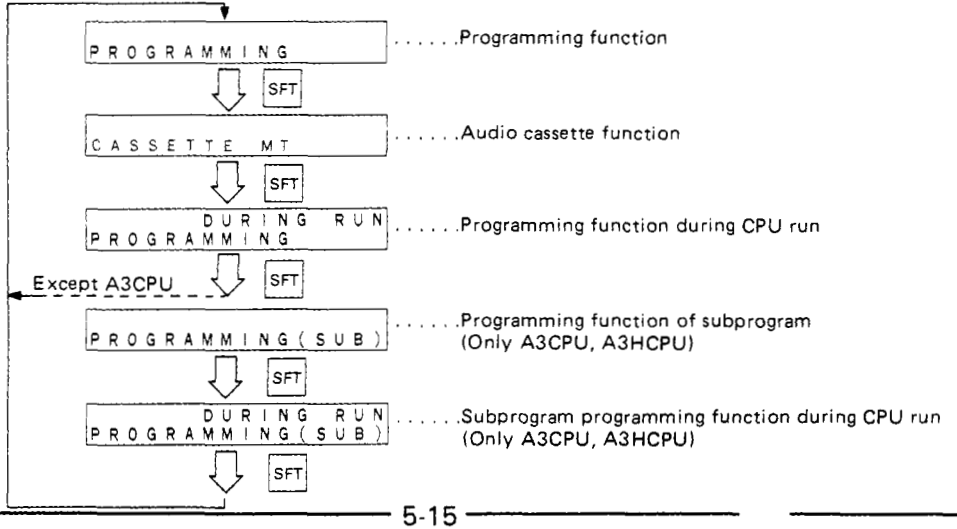
(Programming function is selected.)

Function \ Mode	Verify	Read (Replay)	Write (Record)	Insertion/ Deletion	Monitor	Test	Parameter
PROGRAMMING		Always possible	Only during CPU stop	Only during CPU stop	Always possible	Always possible	Only during CPU stop
CASSETTE MT	Always possible	Only during CPU stop	Always possible				
DURING RUN PROGRAMMING		Always possible	Always possible	Only during CPU stop	Always possible	Always possible	Only during CPU stop
PROGRAMMING(SUB)		Always possible	Only during CPU stop	Only during CPU stop	Always possible	Always possible	Only during CPU stop
DURING RUN PROGRAMMING(SUB)		Always possible	Always possible	Only during CPU stop	Always possible	Always possible	Only during CPU stop

* "Duting CPU stop" means at stop or pause status.

Table 5.1 Operating Conditions of Various Modes

Select either the programming function or the audio cassette function.
By pressing the SFT key, the display screen changes as shown below. By the input of STP +/- key, the screen display function is selected.



5.6 Reset Operation

Operation Procedure

Press both the [RST 0] and [STP +] keys at the same time.

This triggers a hardware reset for the PU. Proceed to Section 5.3.

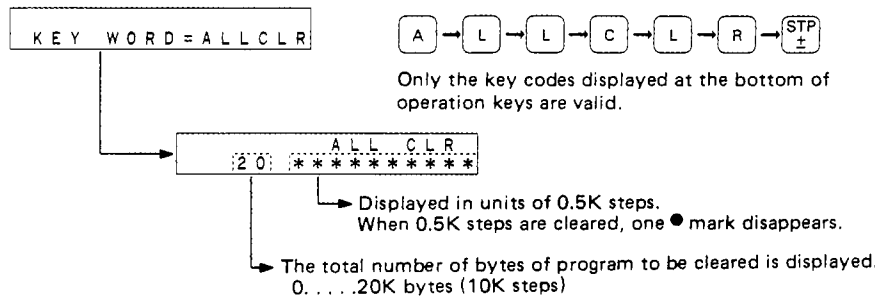
POINT

1) **The reset operation may be used at any time.**
2) **When switching between the programming function and the audio cassette function it is necessary to reset.**

5.7 Clear of Keyword (or Entry Code) and Sequence Program

This section describes the procedure necessary when the entry code has been forgotten. In this case all programs must be cleared.

Operation Procedure


KEY WORD=ALLCLR
A → L → L → C → L → R → STP ±
Only the key codes displayed at the bottom of operation keys are valid.
ALL CLR
20 **********
Displayed in units of 0.5K steps.
When 0.5K steps are cleared, one ● mark disappears.
The total number of bytes of program to be cleared is displayed.
0. . . . .20K bytes (10K steps)

It takes approximately 1.4 seconds to clear 1K bytes (0.5K steps). Upon completion of the clear operation, the buzzer is sounded.

IMPORTANT

When the clear operation described is performed, all sequence programs are cleared and the parameters changed to default values.

6. PROGRAMMING FUNCTION OPERATION PROCEDURES

The following six programming functions are available:

Programming function

- Read . . . . . .For reading a program by step number, instruction, device number, etc.
- Write . . . . . .For writing a program. Programs may be written to the CPU while it is running.
- Insert/delete . . . . . .For inserting and deleting instructions.
- Monitor . . . . . .For monitoring the specified device number, data register, offline switch, etc.
- Test. . . . . .For forcing devices ON/OFF, changing the present value of data registers, switching devices ON/OFF line, checking of programs, reading step numbers of errors and reading/writing of programs in machine code.
- Parameter setting . . . .Mode to set the parameters of the ACPU.

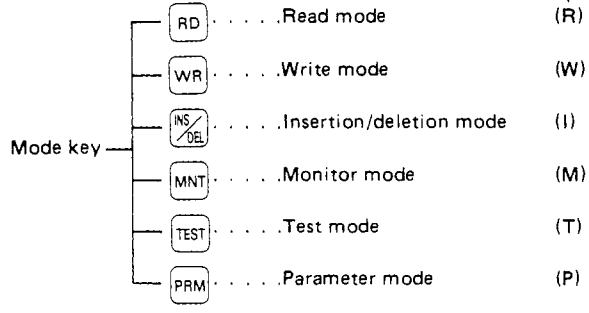
* "During CPU run" means in run status or in step run status.

6.1 Mode Selection

Basic Operation

[Mode key input]

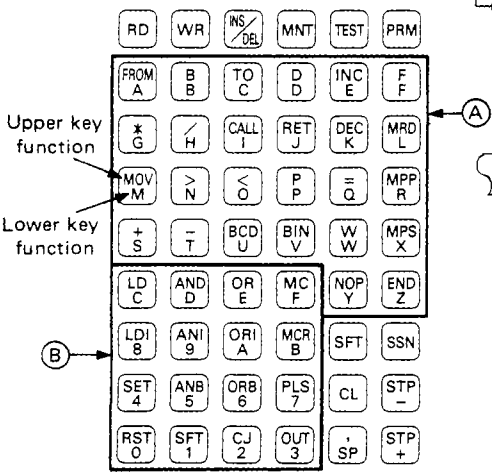
Indicates the abbreviation for the mode displayed at the top left of screen.


Mode key
RD . . . . .Read mode (R)
WR . . . . .Write mode (W)
INS/DEL . . . . .Insertion/deletion mode (I)
MNT . . . . .Monitor mode (M)
TEST . . . . .Test mode (T)
PRM . . . . .Parameter mode (P)

These mode keys may be used at any time during programming.

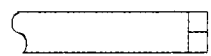
6.2 Screen Display and General Operation Procedure

(1) Mode and indication of key operation

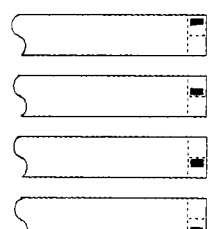


The selected mode is displayed.
During communication with ACPU, the cursor flickers.

Valid key display
When a mode other than parameter mode has been selected, the valid operation for use of the keys is indicated.



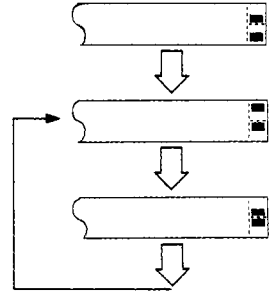
Display example


The upper key functions in area A are valid.
The lower key functions in area A are valid.
The upper key functions in area B are valid.
The lower key functions in area B are valid.

(2) Handling of [SFT] key

The control and display of valid keys is automatically performed by the PU. However, when it is necessary to change this, press the shift (SFT) key.

By pressing the shift key, the key operations change as shown below. (The ⇩ mark indicates a [SFT] key operation.)



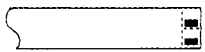
(3) Use of [CL] key

(a) For modes other than parameter mode.

The CL (or CLEAR) key is used to delete an instruction while it is being keyed in. Hence if an error is made during program writing, pressing the CL key will allow the operation to be repeated correctly.

(b) In parameter mode
Processing is stopped.

(4) [SSN] key
This key is used to declare a step number.
When the [SSN] key is pressed, the display of key operation changes to the following.



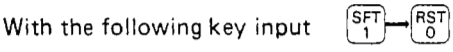
(5) [STP +] and [STP −] keys
These keys are pressed at the end of a series of key operations in order to execute those key operations. After checking the display, press the relevant key.
In this manual, [STP ±] indicates that either of [STP +] or [STP −] key may be pressed.

(6) Cursor display method
The cursor is controlled by the PU and flickers (at intervals of approximately 0.5 seconds). The cursor may appear as ■ or □ depending on the circumstances. In this manual, a frame (□) is used to indicate the cursor position.

(7) Display of key-input data

Key-input data is displayed on the left of the cursor display in due order.

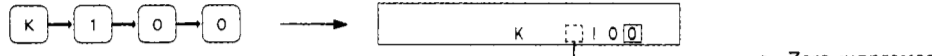
Example:

With the following key input 

0 and ■ are alternately displayed at the cursor position.

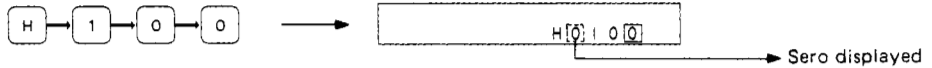
(8) Numeral display

- A decimal number is displayed with zero suppression.

Example: 

- A hexadecimal number is displayed in 4 digits or 8 digits without zero suppression.

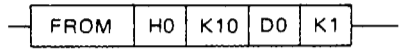
Example:

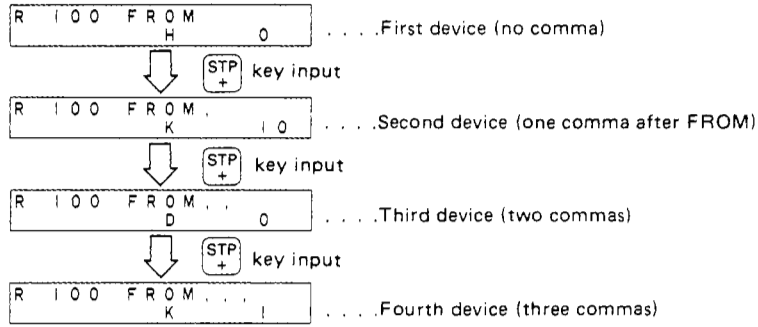


(9) Device display

When there are two or more devices in a basic instruction a comma is provided after the instruction to indicate which of the devices is currently displayed in the lower portion of the screen.

Example:

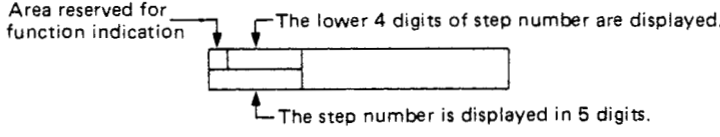

FROM
H0
K10
D0
K1


R 100 FROM H 0
. . . .First device (no comma)
STP + key input
R 100 FROM, K 10
. . . .Second device (one comma after FROM)
STP + key input
R 100 FROM,, D 0
. . . .Third device (two commas)
STP + key input
R 100 FROM,,, K 1
. . . .Fourth device (three commas)

(10) Step number display

Step numbers are displayed in decimal.

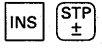
When two five figure step numbers are being displayed they appear as shown on the right.


Area reserved for function indication
The lower 4 digits of step number are displayed.
The step number is displayed in 5 digits.

6.3 Instruction Input Procedures

Instruction input procedures with the PU are classified into four as follows:

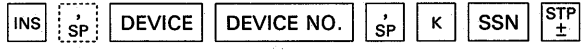
(1) Instruction code only



(2) LD, LDI, AND, ANI, OR, ORI, OUT (except OUT T/C), SFT, SET, RST, PLS, and MCR instructions

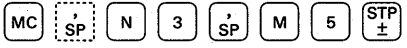
Example: LD X0 ⟶

(3) OUT T/C instruction and MC instruction



Example: OUT T0 K10 ⟶

MC N3 M5 ⟶



REMARKS

In the above instruction input, the input of [SP] key can be omitted.

(4) Instructions other than the above

Press the [SP] key between the instruction and device and between source data and destination data.

Example: MOV K255 D0 ⟶ [MOV] [SP] [K] [2] [5] [5] [SP] [D] [0] [STP ±]

+ D1 D2 D3 ⟶ [+] [SP] [D] [1] [SP] [D] [2] [SP] [D] [3] [STP ±]

DMOVP D1 D2 ⟶ [D] [MOV] [P] [SP] [D] [1] [SP] [D] [2] [STP ±]

or [SFT] [D] [M] [O] [V] [P] [SP] [D] [1] [SP] [D] [2] [STP ±]

(5) ASCII character input procedure

To include a blank code in an ASCII character string, press the [SFT] key.

(6) Handling of devices M and L

In test, monitor, write, and insert modes, the displays of devices M and L change depending on the setting.

Example: Assume that the parameter setting is M0 to 999 and L1000 to L2047.
By pressing the [WR] , [SSN] , [0] , [STP +] , [LD] , [L] , [0] , and [STP +] keys, the PU display shows LD M0.

6.4 Write Mode

Write mode is used to write a new program to the RAM of the programmable controller CPU or modify a program. For write operation in machine language, refer to Section 6.8.6 (page 6-70).

(1) Write during run

Write during CPU run may be performed with the following restrictions:

(a) Any previous instruction which is being overwritten should be of the same length (i.e. same number of steps) as that replacing it.

(b) Both the instruction prior to the write operation and the instruction to be written should not be P or I instructions.

(2) Check for the same coil

In write mode, double coil error check is not made.

Check for double coil may be made in test mode. For the operation procedure and other details, refer to Section 6.8.4 (page 6-67).

(3) Sequence program capacity

When the sequence program capacity is set to nK steps, the number of usable steps is as described below:

0 to (n x 1024 – 2) steps

Example: In the case of 2K steps

0 to 2 x 1024 – 2 = 0 to 2046 (= 2047 steps)

When microcomputer program capacity has been set to mK bytes with the A0J2CPU, the number of steps is 0 to [(7 – m/2) x 1024 – 1)] steps.

Example: Setting of microcomputer program capacity to 2K bytes

0 to [(7 – 2/2) x 1024 – 1] = 0 to 6143 (= 6144 steps)

The relation between the RUN/STOP key switch positions of CPU unit and the write conditions is as indicated below.

Function	Key Switch Position of CPU Unit			
	RUN	STOP	PAUSE	STEP RUN
Programming function	X	○	○	X
Programming function during CPU run	○	○	○	○

REMARKS

For the A0J2CPU, PAUSE and STEP RUN are not available.

○ mark: Write enabled
X mark: Write disabled

The basic operation in write mode is as described below.

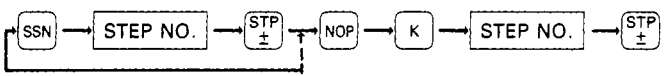
Mode	Item	Basic Operation
Write	All clear (Batch write of NOP)	In write mode: SSN → STEP NO. → STP ± → NOP → K → STEP NO. → STP ± (STEP NO. → STP ± loops back) In read, insert/delete, or monitor mode: Instruction display operation in read, insert/delete, or monitor mode → WR
	Write of program	In write mode: SSN → STEP NO. → STP ± → Setting of instruction → STP ± (STEP NO. → STP ± loops back) In read, insert/delete, or monitor mode: Instruction display operation in read, insert/delete, or monitor mode → WR

- - → indicates operation to be performed when step number is displayed.

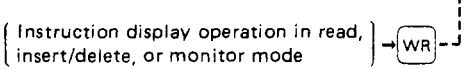
6.4.1 All clear (Consecutive write of NOP)

Basic Operation

- Operation in write mode



- Operation from read, insert/delete, or monitor mode



- - → indicates operation to be performed when step number is displayed.

(1) The memory is cleared using this procedure.

(2) Press the [SSN], [STEP NO.], and [STP ±] keys to display the head step number at which the NOP instructions will be written. By pressing the [NOP], [K], [STEP NO.], and [STP ±] keys, the final step number is specified and the NOP write operation is executed.

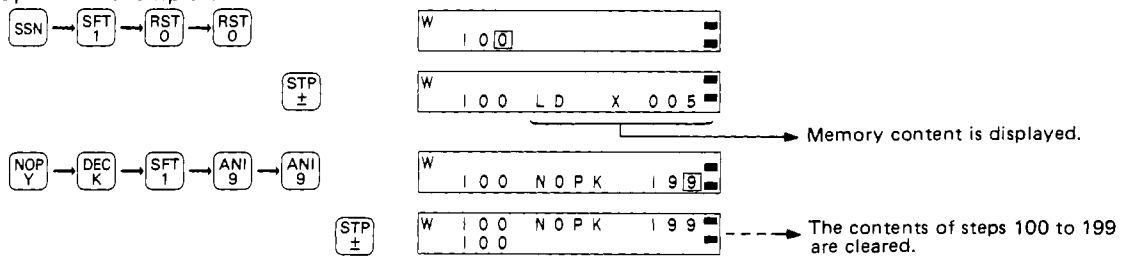
In the operation from read, insert/delete, or monitor mode, the displayed step number is used as a head step number. By pressing the [WR], [NOP], [STEP NO.], and [STP ±] keys, the final step number is specified and the NOP write operation is executed.

If the initial step number is located halfway through an instruction, the head step of that instruction is taken as the head step number.
If the final step number is located halfway through an instruction, the clearing operation is automatically performed up to the final step of that instruciton.
Refer to Operation example 3.

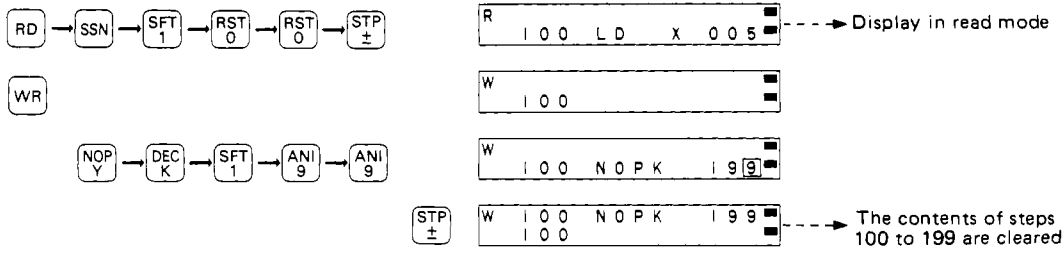
REMARKS

The consecutive write of NOP takes approximately 5.5 seconds per 1K step.

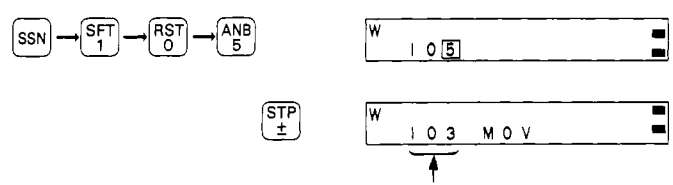
Operation example 1



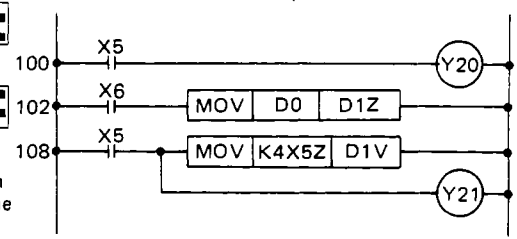
Operation example 2 (Operation from read, insert/delete, or monitor mode)


RD → SSN → SFT 1 → RST 0 → RST 0 → STP ±
R
I 0 0 LD X 0 0 5
Display in read mode
WR
W
I 0 0
NOP Y → DEC K → SFT 1 → ANI 9 → ANI 9
W
I 0 0 N O P K I 9 9
STP ±
W I 0 0 N O P K I 9 9
I 0 0
The contents of steps 100 to 199 are cleared.

Operation example 3 (The head step number or the final step number is located halfway through an instruction)


SSN
SFT 1
RST 0
ANB 5
W
105
STP ±
W
103 MOV
Since the set step number is located halfway through an instruction, the step number changes to that of the head step (103) of instruction.
NOP Y
DEC K
SFT 1
SFT 1
RST 0
W
103 NOPK 110
STP ±
W 103 NOPK 113
103
Since the set final step is located halfway through an instruction, NOP is written up to the last step (113, MOV K4X5Z D1Z) of that instruction.

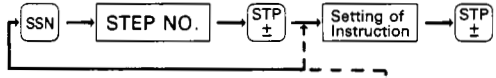
Circuit example



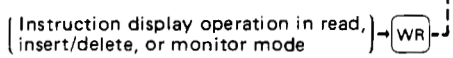
6.4.2 Write of program

Basic Operation

- Operation in write mode

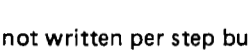


- Operation from read, insert/delete or monitor mode



- - - → indicates operation to be performed when step number is displayed.

(1) After setting the step number, input the instruction and press the [STP ±] key. This writes the instruction to the CPU memory and advances the step number.
Thereafter, each time the [Setting of Instruction] and [STP ±] are input, the instruction is written and the step number incremented.

(2) An instruction is not written per step but written per instruction.
Example:
In the case of 

, MOV, D0, and D1 do not need to be written separately but in blocks.

(3) When the instruction written in the memory is overwritten with another instruction, the number of steps of the preceding instruction may be different from the number of steps of the instruction to be written. In this case, the step numbers of the succeeding program are automatically shifted. (For details, refer to the following page.)
Therefore, if write operation is performed after a program has been written up to the maximum memory capacity, the program in the vicinity of the final step exceeds the memory capacity and is erased.

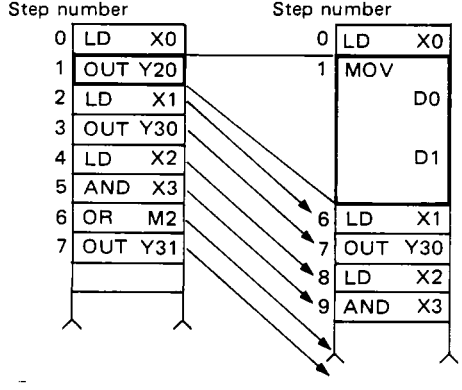
(4) Be sure to write the [END] instruction at the end of program.

Processing examples when the number of steps of the instruction written in the memory is different from the number of steps of the instruction to be written

Example:

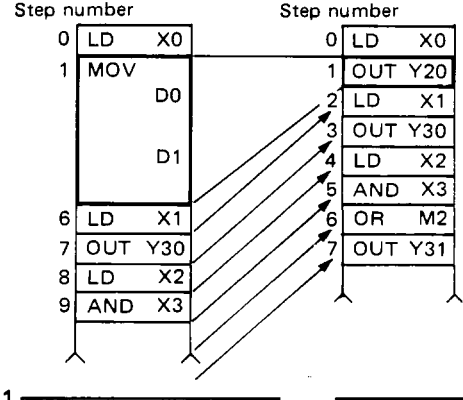
1) To rewrite —(Y20)— (1 step) to

—[MOV D0 D1]— (5 steps)

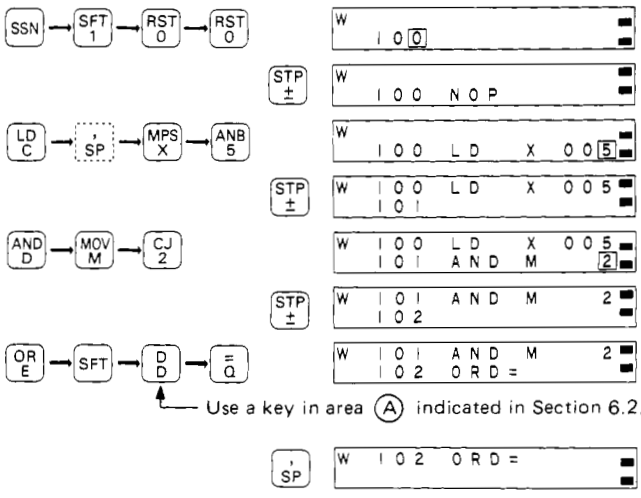


2) To rewrite —[MOV D0 D1]— (5 steps) to

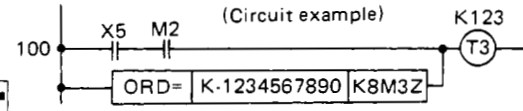
—(Y20)— (1 step)



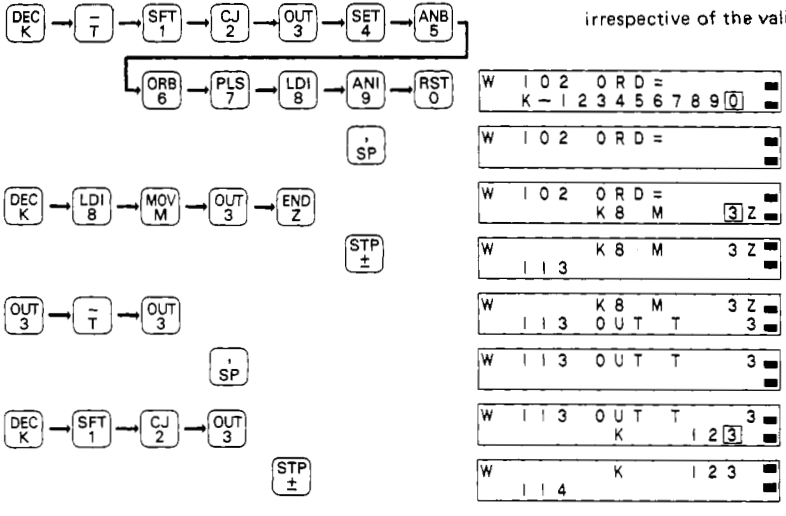
Operation example


SSN
SFT 1
RST 0
RST 0
W
I 0 0
STP ±
W
I 0 0 N O P
. . .The content of step 100 is displayed. (NOP in this example)
LD C
, SP
MPS X
ANB 5
W
I 0 0 L D X 0 0 5
STP ±
W
I 0 0 L D X 0 0 5
I 0 1
. . .Instruction has been written to step 100 and waiting for the input of instruction of step 101.
AND D
MOV M
CJ 2
W
I 0 0 L D X 0 0 5
I 0 1 A N D M 2
STP ±
W
I 0 1 A N D M 2
I 0 2
OR E
SFT
D D
= Q
W
I 0 1 A N D M 2
I 0 2 O R D =
Use a key in area (A) indicated in Section 6.2.
, SP
W
I 0 2 O R D =
. . . . . .By the , SP key input, the display change.

(Circuit example)



The [−/T] key pressed after [K] is regarded as "−" irrespective of the valid key display.


DEC K → −/T → SFT 1 → CJ 2 → OUT 3 → SET 4 → ANB 5
ORB 6 → PLS 7 → LDI 8 → ANI 9 → RST 0
, SP
DEC K → LDI 8 → MOV M → OUT 3 → END Z
STP ±
OUT 3 → −/T → OUT 3
, SP
DEC K → SFT 1 → CJ 2 → OUT 3
STP ±
W I 0 2 0 R D =
K − 1 2 3 4 5 6 7 8 9 0
W I 0 2 0 R D =
W I 0 2 0 R D =
K 8 M 3 Z
W K 8 M 3 Z
I I 3
W K 8 M 3 Z
I I 3 O U T T 3
W I I 3 O U T T 3
W I I 3 O U T T 3
K 1 2 3
W K 1 2 3
I I 4

6.5 Read Mode

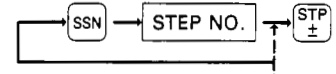
Read mode is used to read the memory of the programmable controller CPU.
The read operation can be performed either during the stop or run of the CPU. However, the read operation during run by instruction or device may take some time. (Time is proportional to the number of steps in the sequence program.)
For the read operation in machine language, refer to Section 6.8.6 (page 6-70).
The basic operation in read mode is as described below.

Mode	Item	Basic Operation
Read	Read by step number	Operation in read mode: SSN → STEP NO. → STP ±
		Operation from write, insert/delete, or monitor mode: (Instruction display operation from write, insert/delete, or monitor mode) → RD → STP ±
	Read by instruction	INS → ' SP → DEVICE → DEVICE NO. → STP ±
	Read by device number	SFT → DEVICE → DEVICE NO. → STP ±

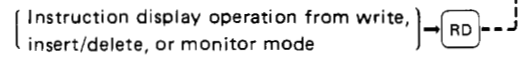
6.5.1 Read by step number

Basic Operation

• Operation in read mode



• Operation from write, insert/delete, or monitor mode



⇢ indicates an operation to be performed when the step number is displayed.

(1) After specifying the step number press the [STP +] or [STP −] to display that instruction.

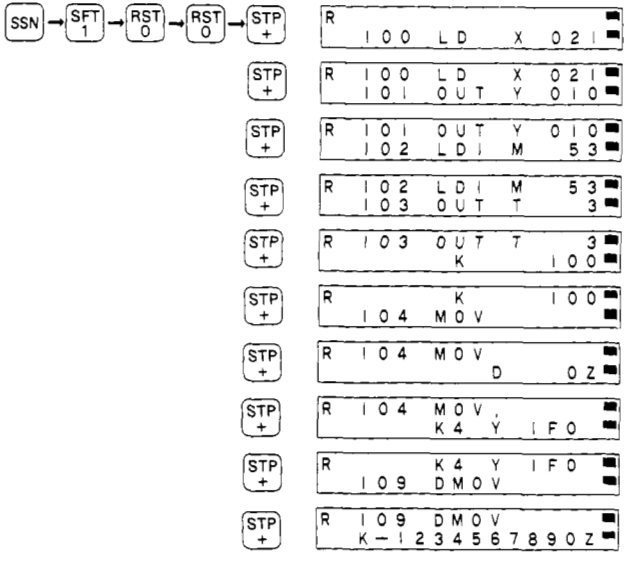
(2) When the specified step number is located halfway through an instruction, the head step number of that instruction is used.

Example: When step 106 is specified in the example shown on the following page, the program is displayed beginning with step 104.

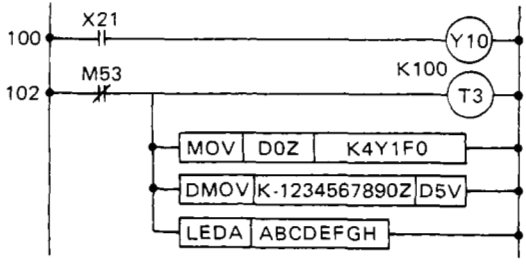
(3) Each time the [STP +] key is pressed, the next instruction is displayed. Each time the [STP −] key is pressed, the preceding instruction is displayed.

(4) If the specified step number exceeds the final step, the program automatically returns step 0.
If the step number precedes step 0, the program automatically returns to the final step.

Operation example



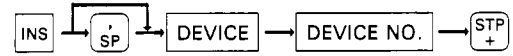
Circuit example



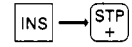
6.5.2 Read by instruction

Basic Operation

- Operation to read instruction with device and device number



- Operation to read only by instruction



(1) The following instructions are read with devices and device numbers provided. The other instructions are read only by instruction.

LD OR AND SET PLS SFT OUT MC
LDI ORI ANI RST MCR

- The OUT T, OUT C, and MC instructions are read as follows:

Example: Instruction. . . . .OUT T0 K123, read as OUT T0 and instruction MC N3 M1023, read as MC N3

- As for the P and I instructions, only read by device number can be performed. (Refer to Section 6.5.3)

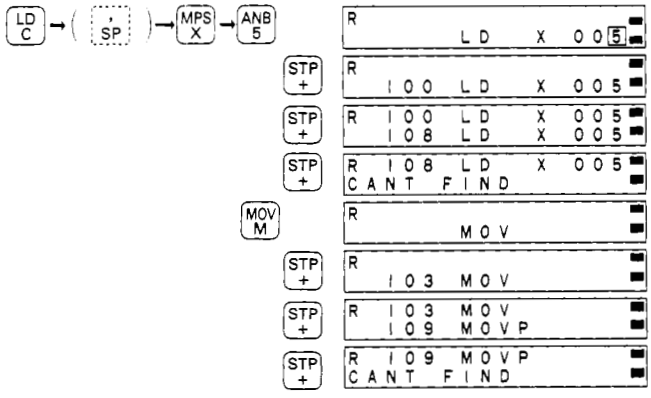
(2) After setting the instruction, the first [STP ±] input searches that instruction, starting at step 0, and displays the detected step. Thereafter, the [STP ±] input starts the search from the next step and displays the next detected step. When the step is not found, "CANT FIND" is displayed.

(3) Change of input data

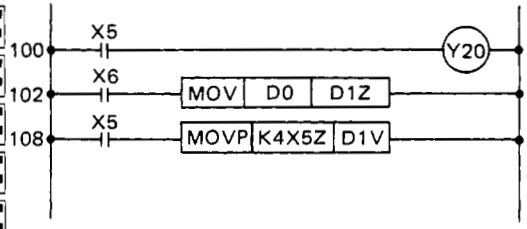
Prior to the [STP ±] input, data can be changed by the following operation.

1) After pressing the [CL] key, input correct data.
2) To change the [INS], input [SFT] and [INS]
3) To change the [DEVICE] and [DEVICE NO.], simply key in the correct data.

Operation example



Circuit example



.....When the MOV instruction is searched, the MOVP instruction is also searched.

Read Procedure by Instruction

(1) Read of comparison instruction
When an instruction has been specified, the specified instruction and all-related instructions are read depending on instructions.

Specified Instruction	Read Instruction		
=	LD=	, AND=	, OR=
D=	LDD=	, ANDD=	, ORD=
< >	LD< >	, AND< >	, OR< >
D< >	LDD< >	, ANDD< >	, ORD< >
>	LD>	, AND>	, OR>
D>	LDD>	, ANDD>	, ORD>
< =	LD< =	, AND< =	, OR< =
D< =	LDD< =	, ANDD< =	, ORD< =
<	LD<	, AND<	, OR<
D<	LDD<	, ANDD<	, ORD<
> =	LD> =	, AND> =	, OR> =
D> =	LDD> =	, ANDD> =	, ORD> =

When the full instruction has been specified (such as LD= and LDD=), only those instructions are searched and read.

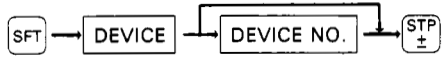
(2) Read of instruction, which is executed when input condition turns on, and instruction which is executed only once when input condition turns on (e.g. MOV and MOVP)

Specified Instruction	Read Instruction
Instruction executed when input condition turns on	• Specified instruction • Instruction executed only once when input condition turns on
Instruction executed only once when input condition turns on	• Specified instruction

For example, in the case of MOV instruction (executed when the input condition turns on) and MOVP instruction (instruction executed only once when the input condition turns on), when MOV is specified, both the MOV instruction and the MOVP instruction are read. When MOVP is specified, only the MOVP instruction is read.

6.5.3 Read by device number

Basic Operation



(1) When a device number is omitted, search is made only by the DEVICE
Devices searched for only by device: Z, V
Devices searched for together with device number: X, Y, M, L, B, F, T, C, D, W, R, A, P, I, N

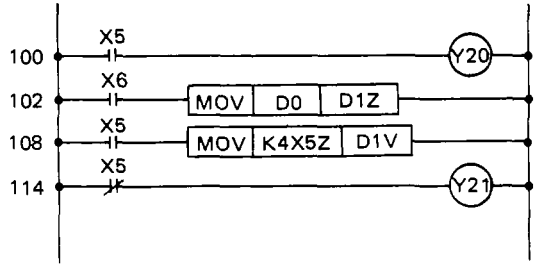
(2) After setting a device and a device number, the first STP ± input searches that device and device number, beginning with step 0, and displays the detected step. Thereafter, the STP ± input initiates search from the next step and displays the detected step.
If the step cannot be detected after searching up to END, "CANT FIND" is displayed.

(3) Change of input data
Prior to the STP ± input, data can be changed with the following operation.
1) Press the CL key and input correct data.
2) Re-input the DEVICE and DEVICE NO. .

Operation example

SFT → MPS X → ANB 5	R X 0 0 5
STP +	R 1 0 0 LD X 0 0 5
STP +	R 1 0 0 LD X 0 0 5 1 0 8 LD X 0 0 5
STP +	R 1 0 9 MOV K 4 X 0 0 5 Z
STP +	R K 4 X 0 0 5 Z 1 1 4 LD I X 0 0 5
STP +	R 1 1 4 LD I X 0 0 5 C A N T F I N D
SFT → END Z	R Z
STP +	R 1 0 2 MOV , D I Z
STP +	R 1 0 9 MOV K 4 X 0 0 5 Z

Circuit example



6.6 Insert/Delete Mode

The insert/delete mode is used to add or delete instructions to or from the program memory. In this mode, operation can be performed only during CPU stop.
The basic operation in insert/delete mode is as described below.

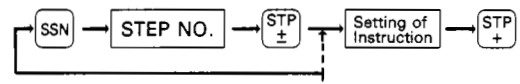
Mode	Item	Basic Operation
Insert/delete	Insertion of instructions	Operation in insert/delete mode: SSN → STEP NO. → STP (±) → Setting of instruction → STP (+) Operation from read, write, or monitor mode: Instruction display operation in read, write, or monitor mode → INS/DEL
	Deletion of instructions	Operation in insert/delete mode: SSN → STEP NO. → STP (±) → STP (−) Operation from read, write, or monitor mode: Instruction display operation in read, write, or monitor mode → INS/DEL

- - → indicates operation to be performed when step number is displayed.

6.6.1 Insertion of instructions

Basic Operation

- Operation in insert/delete mode



- Operation from read, write, or monitor mode

– – → indicates operation to be performed when step number is displayed.

(1) A new program is inserted in front of the specified step. The succeeding instructions and step numbers are adjusted accordingly.
If the insert operation is performed with program lengths approaching the maximum memory capacity and the addition of steps causes the memory capacity to be exceeded, the final instructions will be lost.

(2) An instruction is not inserted per step but per instruction.

(3) After inputting the [STEP NO.], either the [STP +] or [STP −] key may be operated. However, after setting an instruction, it is inserted by pressing [STP +] key. (The [STP −] key is valid in delete mode.)

(4) Instructions are keyed in as described in section 6.3.

(5) When the step number is located halfway through an instruction, the head step number of the instruction is searched and that step number and instruction are displayed.

Operation example

SSN → SFT 1 → RST 0 → SFT 1

```
I
  I 0 □
```

STP ±

```
I
  I 0 1  O U T  Y  0 2 0
```

Displays the program at step 101.

AND D → MOV M → ANB 5

```
I
  I 0 1  A N D  M  5
```

STP +

```
I
  I 0 1  A N D  M  5
  I 0 2
```

.....By STP + input, step 101 and succeeding steps are shifted and the instruction is inserted into step 101.

ANI 9 → MOV M → ORB 6

```
I
  I 0 1  A N D  M  5
  I 0 2  A N I  M  6
```

STP +

```
I
  I 0 2  A N I  M  6
  I 0 3
```

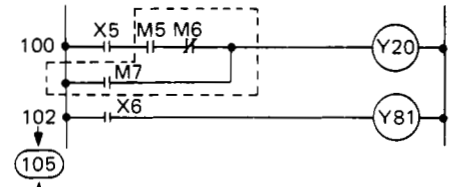
OR E → MOV M → PLS 7

```
I
  I 0 2  A N I  M  6
  I 0 3  O R    M  7
```

STP +

```
I
  I 0 3  O R    M  7
  I 0 4
```

(Circuit example)
In this example, the dotted-line area is inserted.

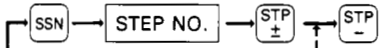


By the insertion operation, the step numbers change.

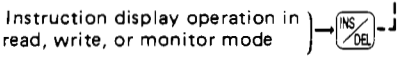
6.6.2 Deletion of instructions

Basic Operation

- Operation in insert/delete mode



- Operation from read, write, or monitor mode



- - → indicates operation to be performed when step number is displayed.

(1) By the input of STP −, the instruction at the displayed step number is deleted. Step numbers are adjusted accordingly.

(2) An instruction is not deleted per step but per instruction.

(3) After inputting the STEP NO., either the STP + or STP − key may be operated. In delete mode, however, only the input of STP − is valid. (The STP + key is valid in insert mode.)

(4) When the step number is located halfway through an instruction, the head step number of the instruction is searched and that step number and instruction are displayed.

Operation example

SSN → SFT 1 → RST 0 → SFT 1

```
I
  1 0 1
```

STP ±

```
I
  1 0 1  A N D  M  5
```

By STP ± input, the instruction at step 101 is displayed.

STP −

```
I
  1 0 1  A N I  M  6
```

By Pressing STP −, AND M5 is deleted and the remaining program steps are shifted ANI M6 is displayed as the instruction at step 101.

STP −

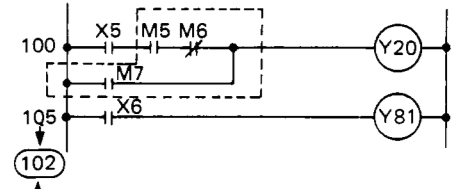
```
I
  1 0 1  O R  M  7
```

STP −

```
I
  1 0 1  O U T  Y  2 0
```

(Circuit example)

In this example, dotted-line area is deleted.



By the deletion operation, the step numbers change.

6.7 Monitor Mode

Monitor mode is used to monitor the ON/OFF states of various devices and the contents of various registers in order to check the operation of the program. Monitor mode can be operated during CPU run. The basic operation in monitor mode is as described below.

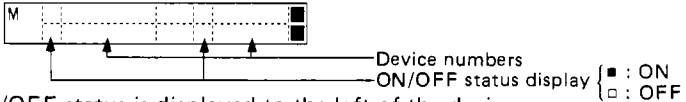
Mode	Item	Basic Operation
Monitor	Monitor of X, Y, M, L, B, and F	DEVICE → DEVICE NO. → STP ±
	Monitor of D, W, R, A, Z, and V	Monitor of D, W, R, and A: DEVICE → DEVICE NO. → STP ± Monitor of Z and V: DEVICE → STP ±
	Monitor of T/C present value and contact ON/OFF status	DEVICE → DEVICE NO. → STP ±
	Continuity check	Operation in monitor mode: SSN → STEP NO. → STP ± (---→) Operation from write, insert/delete, or read mode: (Instruction display operation in write insert/delete, or read mode) → MNT (---→)
	Monitor of offline switch (Y, M, L, B, F)	DEVICE → SFT → DEVICE NO. → STP ± Not available for A0J2, A3HCPU.

---→ indicates operation to be performed when step number is displayed.

6.7.1 Monitor of X, Y, M, L, B, and F

Basic Operation: DEVICE → DEVICE NO. → STP ±

(1) The ON/OFF status of the specified device is displayed.



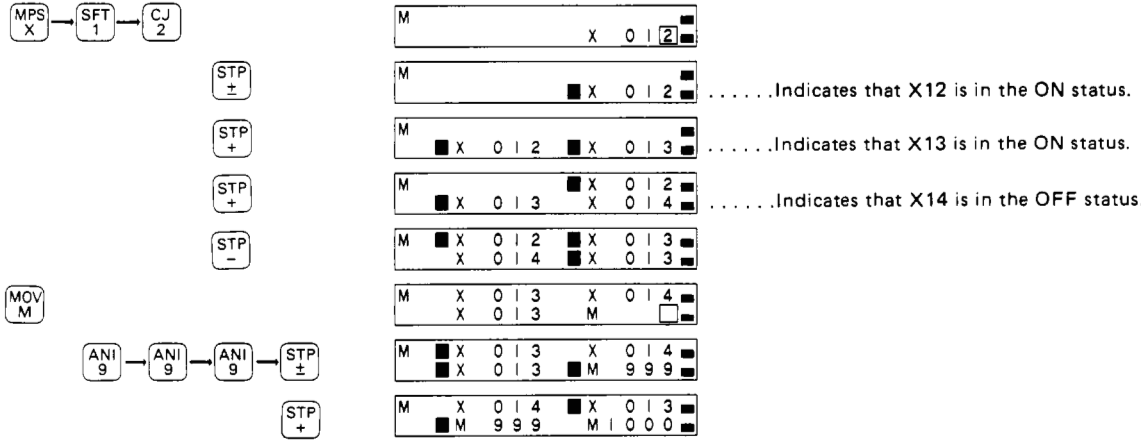
The ON/OFF status is displayed to the left of the device.

(2) By the input of STP +, the ON/OFF status of the next device number is displayed. By the input of STP −, the ON/OFF status of the preceding device number is displayed.
(If STP + is input when the largest device number is being displayed, the device number returns to the head device number. If STP − is input when the head device number is being displayed, the device number returns to the largest device number.)

(3) The screen displays the ON/OFF states of a maximum of four devices.

(4) When the SFT key is pressed during the operation of this function, the execution proceeds to the monitor operation of offline switch (Section 6.7.5 on page 6-54). (Invalid for A0J2, A3HCPU.)

Operation example

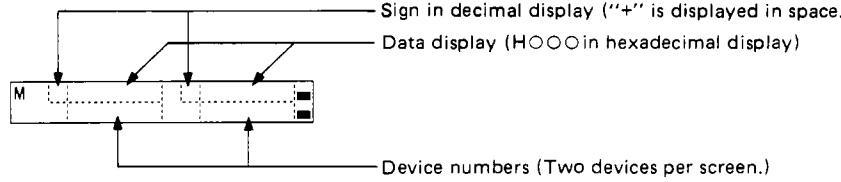

MPS X → SFT 1 → CJ 2
STP ±
STP +
STP +
STP −
MOV M
ANI 9 → ANI 9 → ANI 9 → STP ±
STP +
M X 0 1 2
M X 0 1 2 ■X 0 1 3 .....Indicates that X12 is in the ON status.
M ■X 0 1 2 ■X 0 1 3 .....Indicates that X13 is in the ON status.
M ■X 0 1 3 ■X 0 1 2 X 0 1 4 .....Indicates that X14 is in the OFF status.
M ■X 0 1 2 ■X 0 1 3 X 0 1 4 ■X 0 1 3
M X 0 1 3 X 0 1 4 X 0 1 3 M □
M ■X 0 1 3 X 0 1 4 ■X 0 1 3 ■M 9 9 9
M X 0 1 4 ■X 0 1 3 ■M 9 9 9 M 1 0 0 0

6.7.2 Monitor of D, W, R, A, Z, and V

Basic Operation

- Monitor of D, W, R, and A: DEVICE → DEVICE NO. → STP ±
- Monitor of Z and V: DEVICE → STP ±

(1) The value of the selected device is displayed in decimal or hexadecimal. Perform switching between decimal and hexadecimal with the SFT key after STP ± .


Sign in decimal display ("+" is displayed in space.)
Data display (H○○○in hexadecimal display)
M
Device numbers (Two devices per screen.)

(2) By pressing the [STP +] key, the ON/OFF status of the next device number is displayed. By pressing the [STP −] key, the ON/OFF status of the preceding device number is displayed.
(If [STP +] is input when the largest device number is being displayed, the device number returns to the head device number. If [STP −] is input when the head device number is being displayed, the device number returns to the largest device number.)

(3) The screen displays the contents of two devices.

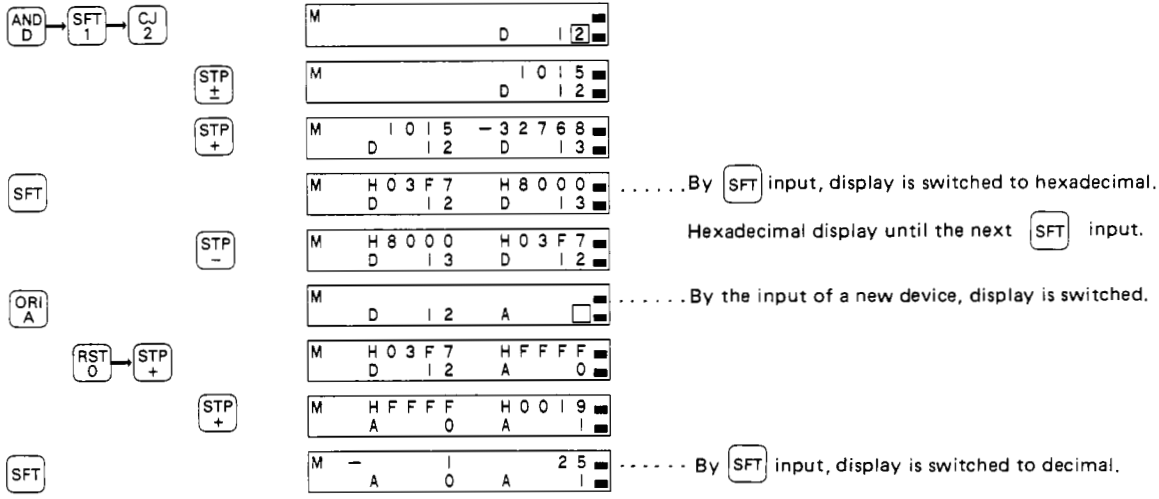
(4) Monitor operation for 32-bit instruction.
The PU monitors device values in units of 16 bits. Therefore, when a 32-bit instruction in used, monitor the contents of the two consecutive devices used fot the 32 bit data instruction.

Example: Contents of registers after the execution of DMOV K100 D0

Decimal monitor	Hexadecimal monitor
D0 = 100	M0064
D1 = 0	M0000

In hexadecimal, the content is H00000064.

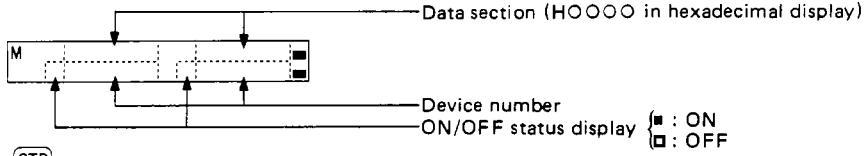
Operation example


AND D → SFT 1 → CJ 2
M D I 2
STP ±
M I 0 I 5 D I 2
STP +
M I 0 I 5 −32768 D I 2 D I 3
SFT
M H 0 3 F 7 H 8 0 0 0 D I 2 D I 3
..... By SFT input, display is switched to hexadecimal.
STP −
M H 8 0 0 0 H 0 3 F 7 D I 3 D I 2
Hexadecimal display until the next SFT input.
ORI A
M D I 2 A
..... By the input of a new device, display is switched.
RST 0 → STP +
M H 0 3 F 7 H F F F F D I 2 A 0
STP +
M H F F F F H 0 0 I 9 A 0 A I
SFT
M − I 25 A 0 A I
------ By SFT input, display is switched to decimal.

6.7.3 Monitor of T/C present value and contact ON/OFF status

Basic Operation: DEVICE → DEVICE NO. → STP ±

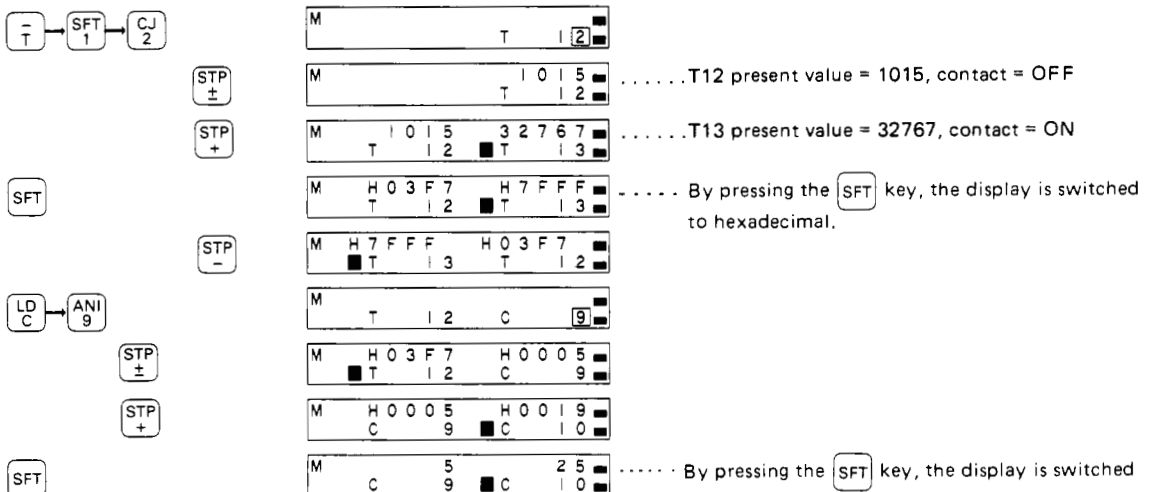
(1) The contact ON/OFF status and content (present value) of the specified device are displayed. Switch between the decimal and hexadecimal with the SFT key after STP ± .



(2) By pressing the STP + key, the ON/OFF status of the next device number is displayed. By pressing the STP − key, the ON/OFF status of the preceding device number is displayed.
(If STP + is input when the largest device number is being displayed, the device number returns to the head device number. If STP − is input when the head device number is being displayed, the device number returns to the largest device number.)

(3) The screen displays the ON/OFF states and values of two devices.

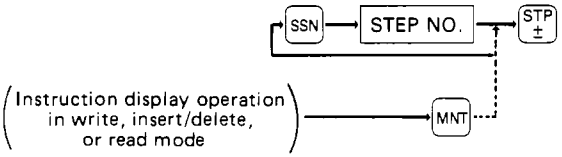
Operation example


(-) T
SFT 1
CJ 2
M T I2
STP ±
M T I2 1015
.....T12 present value = 1015, contact = OFF
STP +
M T I2 32767 T I3
.....T13 present value = 32767, contact = ON
SFT
M T I2 H03F7 T I3 H7FFF
----- By pressing the SFT key, the display is switched to hexadecimal.
STP −
M T I3 H7FFF T I2 H03F7
LD C
ANI 9
M T I2 C 9
STP ±
M T I2 H03F7 C 9 H0005
STP +
M C 9 H0005 C 10 H0019
SFT
M C 9 5 C 10 25
----- By pressing the SFT key, the display is switched to decimal.

6.7.4 Continuity check

Basic Operation

- Operation in monitor mode
- Operation from write, insert/delete, or read mode



----→ indicates operation to be performed when step number is displayed.

(1) Using the operation "Read by step number" (Section 6.5.1 on page 6-25), a program is read and the continuity status, contact ON/OFF status, and device present value are displayed.

(2) Explanation of display (For display screen, refer to the following page)

Continuity status: The continuity status after the execution of the instruction is displayed to the left of the instruction. (Not displayed for A0J2, A3HCPU)

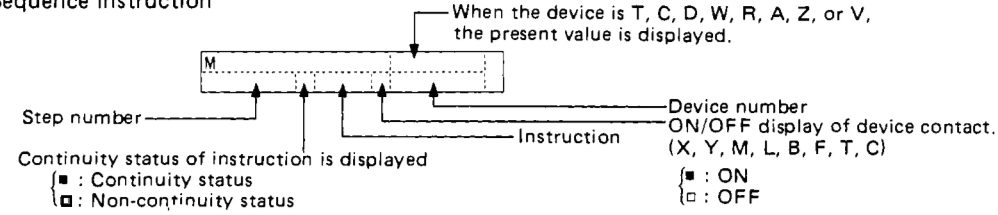
ON/OFF display: Displayed to the left side of the device number.

Present value: Displayed above the T/C number for a sequence instruction.
Displayed to the left of the device number for a basic or application instruction.
Switch between decimal and hexadecimal by pressing the SFT key after STP(+).

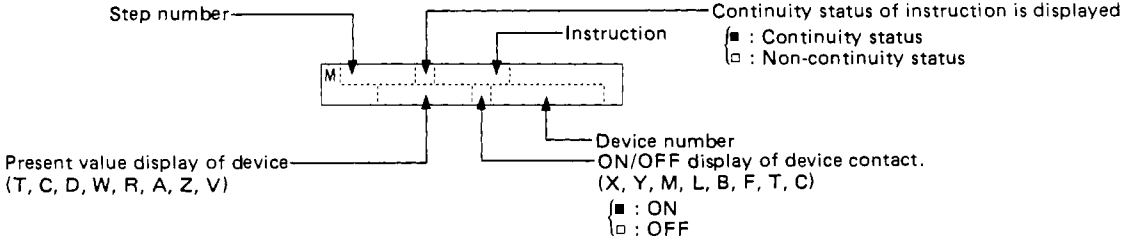
(3) By pressing the STP(+) key, the next instruction is displayed. By pressing the STP(−) key, the preceding instruction is displayed.
(If STP(+) is input at the final number, the step number returns to the head step number. If STP(−) is input at the head step number, the step number returns to the final step number.)

(4) Even if digit qualification or index qualification has been performed, the continuity check is made for the previous device number.
Example D0Z: The present value of D0 is displayed. (Not the present value of D[0+Z])
K2X0: ON/OFF of X0 is displayed. (Not ON/OFF of X0 to X7)

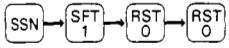
(5) Sequence instruction

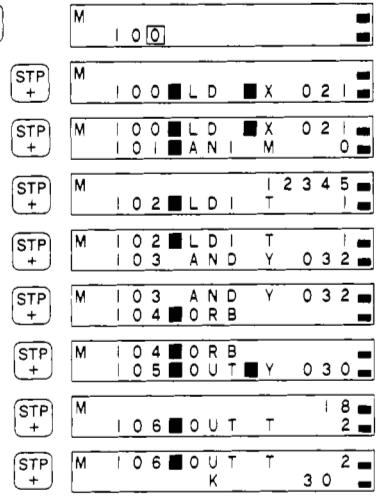

When the device is T, C, D, W, R, A, Z, or V, the present value is displayed.
M
Step number
Continuity status of instruction is displayed
■ : Continuity status
□ : Non-continuity status
Instruction
Device number
ON/OFF display of device contact.
(X, Y, M, L, B, F, T, C)
■ : ON
□ : OFF

(6) Basic instruction and application instruction

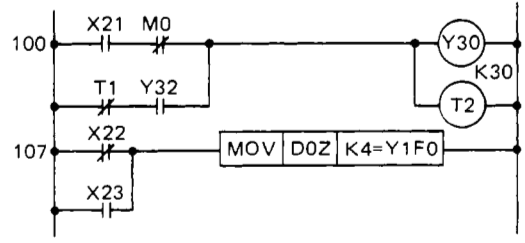

Step number
Continuity status of instruction is displayed
Instruction
■ : Continuity status
□ : Non-continuity status
M
Device number
Present value display of device
(T, C, D, W, R, A, Z, V)
ON/OFF display of device contact.
(X, Y, M, L, B, F, T, C)
■ : ON
□ : OFF

Operation example





(Circuit example)

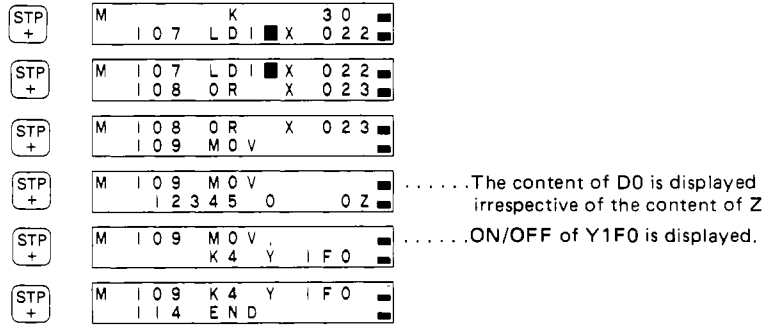


.....T1 has not yet timed up.

.....Since X21 and M0 are in continuity status, the ORB instruction is in continuity status.

.....Y30 is in continuity status.

.....T2 coil is in continuity status. Device T2 is off.



.....The content of D0 is displayed irrespective of the content of Z.

.....ON/OFF of Y1F0 is displayed.

6.7.5 Monitor of offline switch (Y, M, L, B, F) (Not available for A0J2, A3HCPU.)

Basic Operation

DEVICE → SFT → DEVICE NO. → STP (+)

(1) The offline switch status of the selected device is displayed.

Offline status causes the coil of the element to be effectively disconnected from its controlling logic.

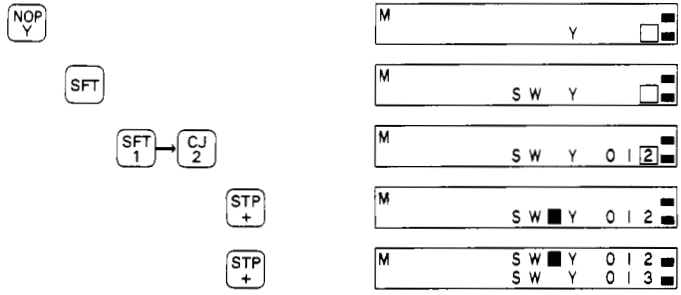
(2) By pressing the STP (+) key, the status of the next device number is displayed. By pressing the STP (−) key, the status of the preceding device number is displayed.
(If STP (+) is input when the largest device number is being displayed, the device number returns to the head device number. If STP (−) is input when the head device number is being displayed, the device number returns to the largest device number.)

(3) The screen displays the offline statuses of two devices.

(4) When the [SFT] key is pressed during the operation of this function, the execution proceeds to the monitor operation of X, Y, M, L, B, and F (Section 6.7.1 on page 6-42).

(5) For the set/reset operation of offline switch, refer to Section 6.8.3. on page 6-64.

Operation example



6.8 Test Mode

Test mode is used to perform the test operation for the program and to read any error steps and error descriptions when appropriate. In test mode, operation can be performed during CPU run or stop.
The basic operation in test mode is as described below.

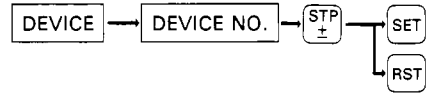
Mode	Item	Basic Operation
Test	Set/reset of X, Y, M, L, B, and F	DEVICE → DEVICE NO. → STP ± → SET (or RST)
	Present value change of T, C, D, W, R, A, Z, and V	DEVICE → DEVICE NO. → STP ± → , → Present value → STP ±
	Set/reset of offline switch (Y, M, L, B, and F)	DEVICE → SFT → DEVICE NO. → STP ± → SET (or RST)
	Program check	P → STP ±
	Read of error step and error description at error time	K → STP ±

Mode	Item	Basic Operation
Test	Read/write in machine language	Read [SSN] → ADDRESS → [STP ±] Write [SSN] → ADDRESS → [STP ±] → Machine language code → [STP ±]

For the A0J2, A3HCPU, set/reset of the offline switch cannot be performed.

6.8.1 Set/reset of X, Y, M, L, B, and F

Basic Operation



(1) The device is turned on by the input of SET 4 and turned off by the input of RST 0 .
When operation is performed during CPU run, the device is merely turned on/off as soon as the set/reset operation is performed from the PU. Thereafter, the status of the device depends on the sequence program.

(2) If the device being set/reset is X, the processing of any instructions using this device is carried out on an "or" basis between the image memory and the actual input. (The image memory is set/reset by this function)
Take care not to SET/RESET X devices used in the data link.

(3) By the input of [STP +], the next device number is displayed. By the input of [STP −], the preceding device number is displayed.
(If [STP +] is input when the largest device number is being displayed, the device number returns to the head device number. If [STP −] is input when the head device number is being displayed, the device number returns to the largest device number.)

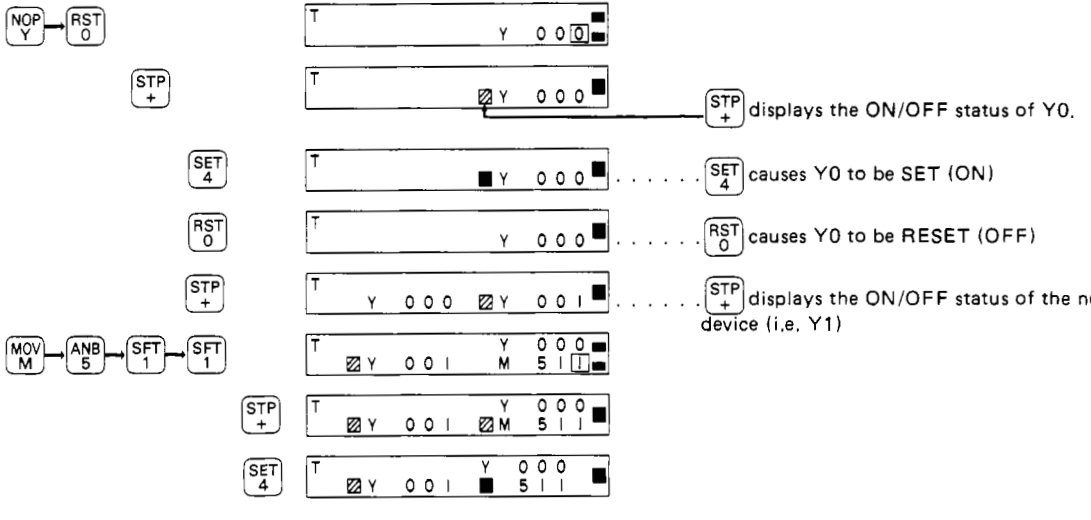
(4) The screen displays the states of a maximum of four devices.

(5) When the [SFT] key is pressed during the operation of this function, the execution proceeds to the set/reset operation of offline switch (Section 6.8.3 on page 6-64). (Invalid for A0J2, A3HCPU)

IMPORTANT

Be sure to reset any device which has been set by this operation. e.g. by use of the RESET switch on the CPU unit.

Operation example



6.8.2 Present value change of T, C, D, W, R, A, Z, and V

Basic Operation

DEVICE → DEVICE NO. → STP ± → , SP → Present value → STP ±

(1) By inputting DEVICE , DEVICE NO. , and STP ± , the current value and ON/OFF status (for T and C) of the selected device number is displayed. Monitor is stopped by the input of , SP , the content of set device number is changed to the input value by the input of Present value and STP ± , and then monitor display is resumed.
To set the present value in hexadecimal, input H and Present value
To set the present value in decimal, input only the Present value
(For the input of present value data, use the device number setting keys in area Ⓑ shown on page 6-3.)
During CPU run, the present value of the device changes according to the normal processing of the program.

(2) Switch between decimal and hexadecimal constants with the SFT key.

(3) When "0" is written as the present value of timer/counter, the contact is also reset.

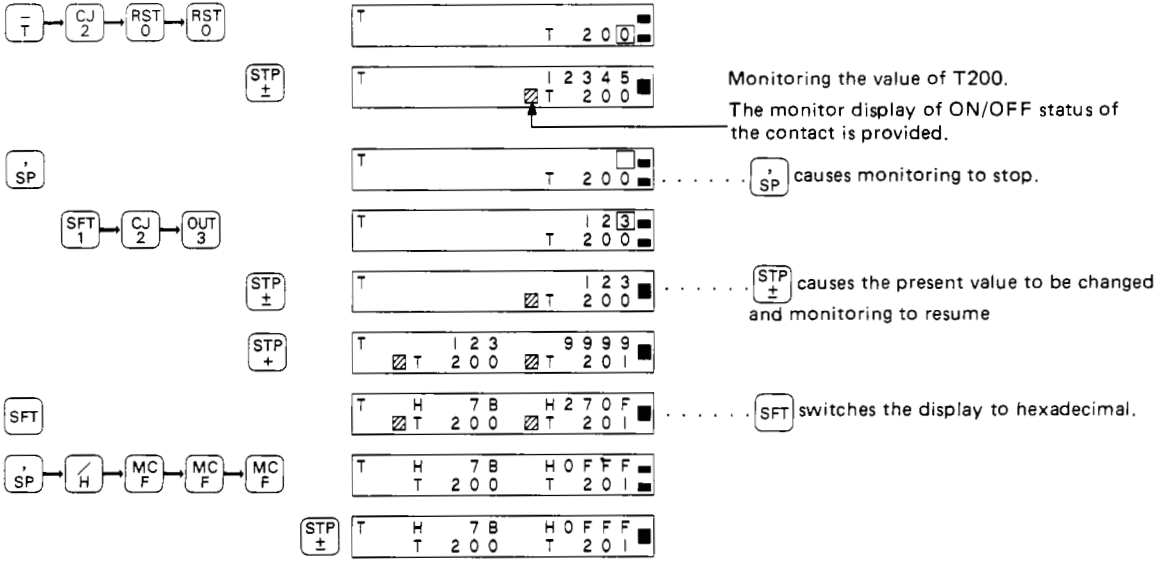
(4) By pressing the [STP +] key, the value of the next device number is displayed. By the input of [STP −], the value of the preceding device number is displayed.
(If [STP +] is input when the largest device number is being displayed, the device number returns to the head device number. If [STP −] is input when the head device number is being displayed, the device number returns to the largest device number.)

(5) The screen displays the contents of two devices.

(6) Present value change of special register
The special register is controlled by the OS of the A series CPU. To change the present value of a special register, perform operation after checking the content, referring to the CPU User's manual.

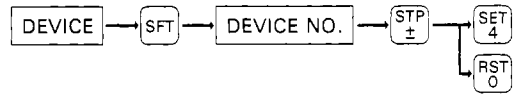
(7) Present value change when 32-bit instruction is used
Changes to present values can only be done in units of 16 bits using the PU. Therefore, convert the 32-bit data to hexadecimal and write it in units of 16 bits.
Example: To store K305432864 (H12348920) to D0 and D1, write H8920 to D0 and H1234 to D1.

Operation example


(−/T) → (CJ/2) → (RST/0) → (RST/0)
T 200 0
(STP/±)
T 12345 T 200
Monitoring the value of T200.
The monitor display of ON/OFF status of the contact is provided.
(,/SP)
T 200
(,/SP) causes monitoring to stop.
(SFT/1) → (CJ/2) → (OUT/3)
T 123 T 200
(STP/±)
T 123 T 200
(STP/±) causes the present value to be changed and monitoring to resume
(STP/+)
T 123 T 200 T 999 T 201
(SFT)
T H 7B T 200 H270F T 201
(SFT) switches the display to hexadecimal.
(,/SP) → (/H) → (MC/F) → (MC/F) → (MC/F)
T H 7B T 200 H0FFF T 201
(STP/±)
T H 7B T 200 H0FFF T 201

6.8.3 Set/reset of offline switch (Y, M, L, B, F) (Not available for A0J2, A3HCPU)

Basic Operation



(1) The selected device number is placed online by pressing [SET 4] and offline by pressing [RST 0].
(In offline status, a device can be set to the on or off status by the operation of Section 6.8.1, without regard to the operation result of sequence program.)

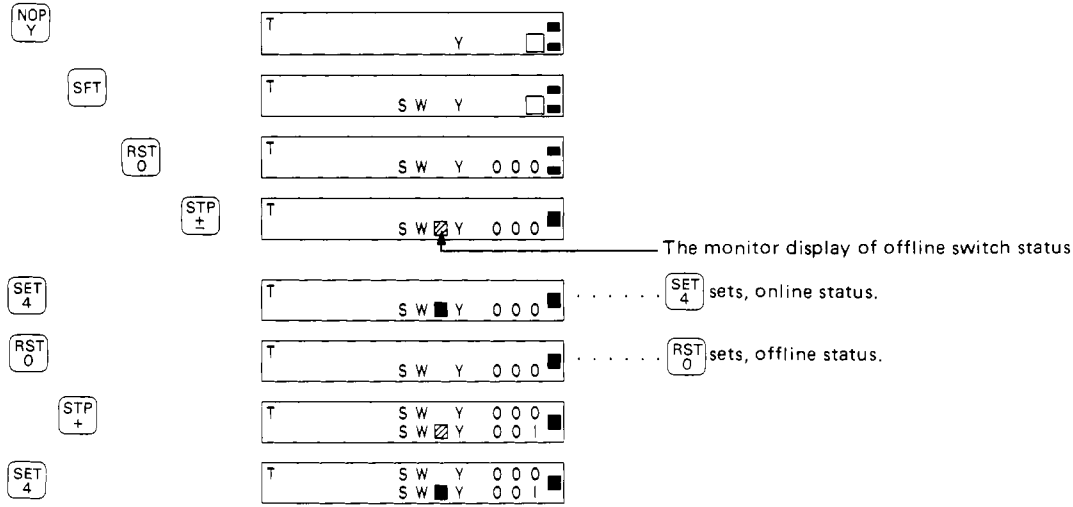
(2) Take care when using this function in conjunction with special function units, since certain Y numbers cannot be set/reset.

(3) By pressing [STP +], the next device number is displayed. By pressing [STP −], the preceding device number is displayed.
(If [STP +] is input when the largest device number is being displayed, the device number returns to the head device number. If [STP −] is input when the head device number is being displayed, the device number returns to the largest device number.)

(4) The screen displays the contents of a maximum of two devices.

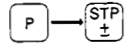
(5) When the SFT key is pressed during the operation of this function, execution proceeds to the set/reset operation of X, Y, M, L, B, and F (Section 6.8.1 on page 6-58).

Operation example



6.8.4 Program check

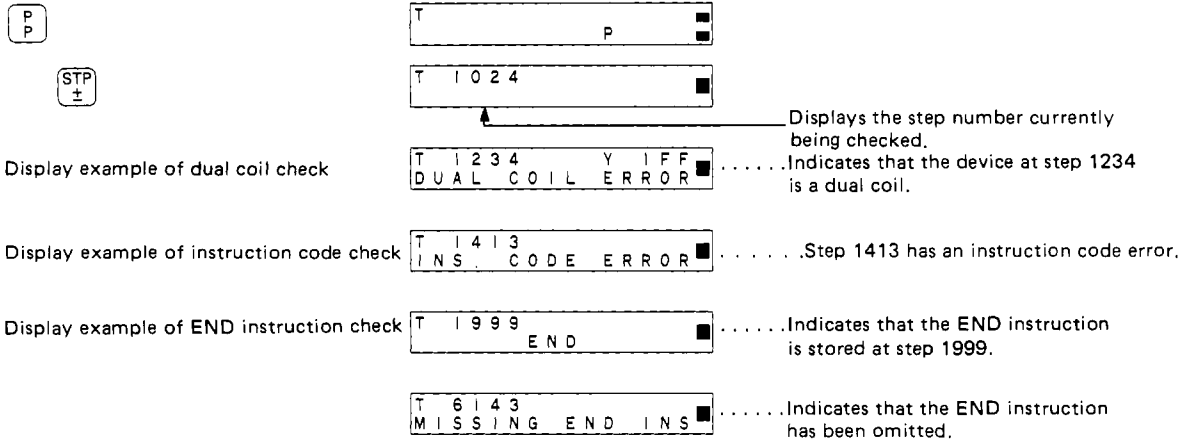
Basic Operation



(1) The sequence program is checked by pressing P and STP ±.
Items which are checked are as follows:
(a) Dual coil check: Devices (Y, M, L, B, F, T, and C) in sequence instructions (OUT, SET, SFT, PLS, MC, and PLF) are checked for dual coils.
(b) Instruction code check: Sequence program instruction codes are checked.
(c) END instruction check: END instruction in sequence program is checked.

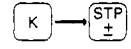
(2) When an error has been found as a result of the check, the step number and an error message are displayed. Checking may be resumed by pressing STP ±, beginning at the next step.
Since all instructions from step 0 to the END instruction are checked, this may take a few seconds.

Operation example

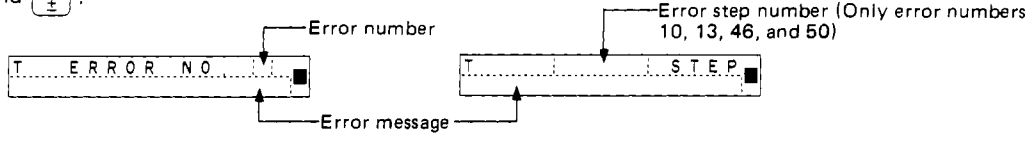


6.8.5 Reading the error step and error description

Basic Operation



(1) An error, which has occurred in the programmable controller CPU, is read and displayed by pressing K and STP ±.



(2) When there is no error, T NO ERROR is displayed.

For error numbers and error messages, refer to Section 8.3 on page 8-7.

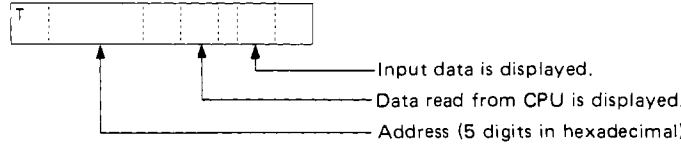
6.8.6 Read/write in machine language

Basic Operation

Read: SSN → ADDRESS → STP (±)

Write: SSN → ADDRESS → STP (±) → Machine language code → STP (±)

(1) The content of address set by SSN, ADDRESS, and STP (±) is directly read from the CPU and displayed in hexadecimal. The new machine language code may then be written to the CPU by inputting Machine language code and STP (±). The read operation can be performed even during CPU run. However, the write operation can be performed only during CPU stop.
If the PU has been set to programming function during CPU run, the write operation can be performed during CPU run.

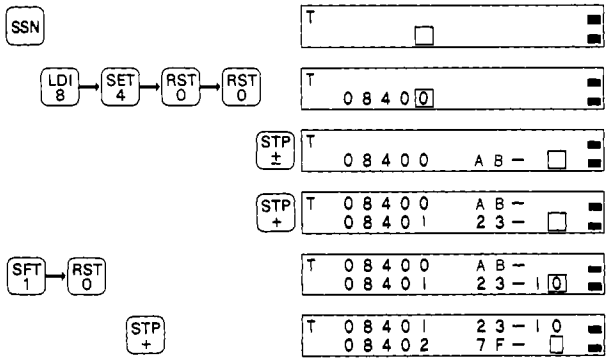


(2) By pressing [STP +] , the content of the next address is displayed. By pressing [STP −] , the content of the previous address is displayed.

REMARKS

In this operation, only the area (B) (device number setting keys) shown on page 6-3 are valid.

Operation example


SSN
T
LDI 8
SET 4
RST 0
RST 0
T 0840 0
STP ±
T 08400 AB–
. . .By pressing STP + , the content of address 8400 (hexadecimal) is displayed.
STP +
T 08400 AB–
08401 23–
. . .By pressing STP ± , the content of the next address is displayed.
SFT 1
RST 0
T 08400 AB–
08401 23– 0
STP +
T 08401 23– 0
08402 7F–
. . .By pressing STP + , 10 (hexadecimal) is written to address 8401 (hexadecimal).

6.9 Parameter Setting Mode

Parameter setting mode is used to set the parameters of the A1, 2 and 3 CPUs. In this mode, operation can be performed only during CPU stop. A list of parameter is indicated in Table 6.1. Some parameters cannot be set using the A7PU, these must be set using the A6GPP or A6HGP.

	CPU / Item	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Memory capacity setting	Main program	3K steps	No setting	6K steps	1 to 6K steps (in units of 1K step)	6K steps	1 to 14K steps (in units of 1K step)	6K steps	1 to 30K steps (in units of 1K step)	6K steps	1 to 30K steps (in units of 1K step)
	Subprogram	0K step	No setting	0K step	No setting	0K step	No setting	0K step	1 to 30K steps (in units of 1K step)	0K step	1 to 30K steps (in units of 1K step)
	File register	0K point	No setting	0K point	No setting	0K point	0 to 4K steps (in units of 1K step)	0K step	0 to 8K steps (in units of 1K step)	0K point	0 to 8K steps (in units of 1K step)

Table 6.1 Default Values and Set Values for Each CPU (Continue)

	Item \ CPU	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Memory capacity setting	Comment capacity	1.5K bytes 95 points	No setting	0K byte	0 point or 128 points	0K byte	0 to 4032 points (in units of 64 points)	0K byte	0 to 4032 points (in units of 64 points)	0K byte	0 to 4032 points (in units of 64 points)
	Sampling trace	Absent	No setting	Absent	No setting	Absent	Present/ absent	Absent	Present/ absent	Absent	Present/ absent
	Status latch	Absent	No setting	Absent	No setting	Absent	Present/ absent	Absent	Present/ absent	Absent	Present/ absent
Latch range setting		Half latch Devices to be latched L1024 to 2047, C64 to 127, D256 to 511, T40 to 79, T100 to 119, T124 to 127, B200 to 3FF (W200 to 3FF)	No latch, half latch, full latch	—	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF (in units of 1 point)	—	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF (in units of 1 point)	—	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF (in units of 1 point)	—	B0 to 3FF T0 to 255 C0 to 255 D0 to 1023 W0 to 3FF (in units of 1 point)

Table 6.1 Default Values and Set Values for Each CPU (Continue)

CPU / Item	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Link range specification	—	No setting	—	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 31F Link register (W): W0 to 3FF Monitor time: 10ms to 2000ms (in units of 10ms)	—	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 31F Link register (W): W0 to 3FF Monitor time: 10ms to 2000ms (in units of 10ms)	—	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 31F Link register (W): W0 to 3FF Monitor time: 10ms to 2000ms (in units of 10ms)	—	Number of link stations: 1 to 64 Input (X): X0 to FF Output (Y): Y0 to FF Link relay (B): B0 to 31F Link register (W): W0 to 3FF Monitor time: 10ms to 2000ms (in units of 10ms)

Table 6.1 Default Values and Set Values for Each CPU (Continue)

	CPU	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
	Item	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Auxiliary function setting	Setting of internal relay, latch relay, step relay	M0 to 999 L1000 to 2047	No setting (depends on latch range setting)	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047	M0 to 999 L1000 to 2047	M/L/S0 to 2047
	Watch dog timer	200ms	No setting	200ms	10ms to 2000ms (in units of 10ms)	200ms	10ms to 2000ms (in units of 10ms)	200ms	10ms to 2000ms (in units of 10ms)	200ms	No Setting
	Timer setting	100ms: T0 to 79 10ms: T80 to 119 integrating T120 to 255	No setting	100ms: T0 to 199 10ms: T200 to 255	Setting of 100ms, 10ms, integrating timers (in units of 8 points)	100ms: T0 to 199 10ms: T200 to 255	Setting of 100ms, 10ms, integrating timers (in units of 8 points)	100ms: T0 to 199 10ms: T200 to 255	Setting of 100ms, 10ms, integrating timers (in units of 8 points)	100ms: T0 to 199 10ms: T200 to 255	Setting of 100ms, 10ms, integrating timers (in units of 8 points)

Table 6.1 Default Values and Set Values for Each CPU (Continue)

CPU / Item		A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Auxiliary function setting	I/O assignment	64 points	No setting	—	0 to 64 points each (in units of 16 points) • input (X) unit • Output (Y) unit • Special function unit • Vacant slot	—	0 to 64 points each (in units of 16 points) • input (X) unit • Output (Y) unit • Special function unit • Vacant slot	—	0 to 64 points each (in units of 16 points) • input (X) unit • Output (Y) unit • Special function unit • Vacant slot	—	0 to 64 points each (in units of 16 points) • input (X) unit • Output (Y) unit • Special function unit • Vacant slot
	Remote RUN/PAUSE setting	—	No setting	—	X0 to FF • Only 1 point can be set for RUN contact • Setting of PAUSE contact alone is not allowed.	—	X0 to FF • Only 1 point can be set for RUN contact • Setting of PAUSE contact alone is not allowed.	—	X0 to FF • Only 1 point can be set for RUN contact • Setting of PAUSE contact alone is not allowed.	—	X0 to FF • Only 1 point can be set for RUN contact • Setting of PAUSE contact alone is not allowed.

Table 6.1 Default Values and Set Values for Each CPU (Continue)

	CPU / Item	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Auxiliary function setting	Run mode at error	Continuation • Fuse blow • Operation error	No setting	(Continuation) • Fuse blow • Operation error [Stop] • I/O unit verify error • Special function unit operation error	(Stop/continuation) • Fuse blow • Operation error • I/O unit verify error • Special function unit operation error	(Continuation) • Fuse blow • Operation error [Stop] • I/O unit verify error • Special function unit operation error	(Stop/continuation) • Fuse blow • Operation error • I/O unit verify error • Special function unit operation error	(Continuation) • Fuse blow • Operation error [Stop] • I/O unit verify error • Special function unit operation error	(Stop/continuation) • Fuse blow • Operation error • I/O unit verify error • Special function unit operation error	(Continuation) • Fuse blow • Operation error [Stop] • I/O unit verify error • Special function unit operation error	(Stop/continuation) • Fuse blow • Operation error • I/O unit verify error • Special function unit operation error
	Annunciator display mode	Absent	No setting	Absent	No setting	Absent	No setting	Absent	Display present/absent	Absent	Display present/absent

Table 6.1 Default Values and Set Values for Each CPU (Continue)

CPU / Item		A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
		Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
Auxiliary function setting	STOP → RUN output mode	Operation status prior to STOP is restored.	No setting	Operation status prior to STOP is restored.	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is restored.	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is restored.	Output of status prior to STOP or result one scan after operation	Operation status prior to STOP is restored.	Output of status prior to STOP or result one scan after operation
	Counter setting Interrupt counter	—	No setting	—	C0 to 247 (in units of 8 points)	—	C0 to 247 (in units of 8 points)	—	C0 to 247 (in units of 8 points)	Absent	No setting
Print title entry		—	128 alphanumeric and special characters	—	128 alphanumeric and special characters	—	128 alphanumeric and special characters	—	128 alphanumeric and special characters	—	128 alphanumeric and special characters
Entry code (keyword) setting		—	No setting	—	6 hexadecimal digits (0 to 9, A to F)	—	6 hexadecimal digits (0 to 9, A to F)	—	6 hexadecimal digits (0 to 9, A to F)	—	6 hexadecimal digits (0 to 9, A to F)

Table 6.1 Default Values and Set Values for Each CPU (Continue)

CPU / Item	A0J2 CPU		A1(E)CPU, A1NCPU		A2(E)CPU, A2NCPU		A3(E)CPU, A3NCPU		A3HCPU	
	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range	Default value	Parameter setting range
I/O control mode	Direct	No setting	A1 direct A1E I/O refresh	No setting	A2 direct A2E I/O refresh	No setting	A3 direct A3E I/O refresh	No setting	I/O direct	• I/O refresh • Input refresh, output direct • Input direct, output refresh • I/O direct
Operation mode	Initial operation	No setting	Initial operation	No setting	Initial operation	No setting	Initial operation	No setting	Initial operation	No setting
Interrupt counters for I0 to I31	Absent	No setting	Absent	No setting	Absent	No setting	Absent	No setting	Absent	Absent/present set per counter

Table 6.1 Default Values and Set Values for Each CPU

Internal relay, latch relay, step relay range setting for the A0J2CPU.

Selection	Unlatched Area	Latched Area
No latch	M0 to 2047, T0 to 255, C0 to 255, D0 to 511, B0 to 3FF, (W0 ~ 3FF)	No setting
Half latch	M0 to 1023, C0 to 63, D0 to 255, T0 to 39, T80 to 99, T120 to 123, B0 to 1FF, (W0 to FF)	L1024 to 2047, C64 to 127, D256 to 511, T40 to 79, T100 to 119, T124 to 127, B200 to 3FF, (W200 to 3FF)
All latch	No setting	L0 to 2047,T0 to 255, C0 to 255, D0 to 511, B0 to 3FF, (W0 to 3FF)

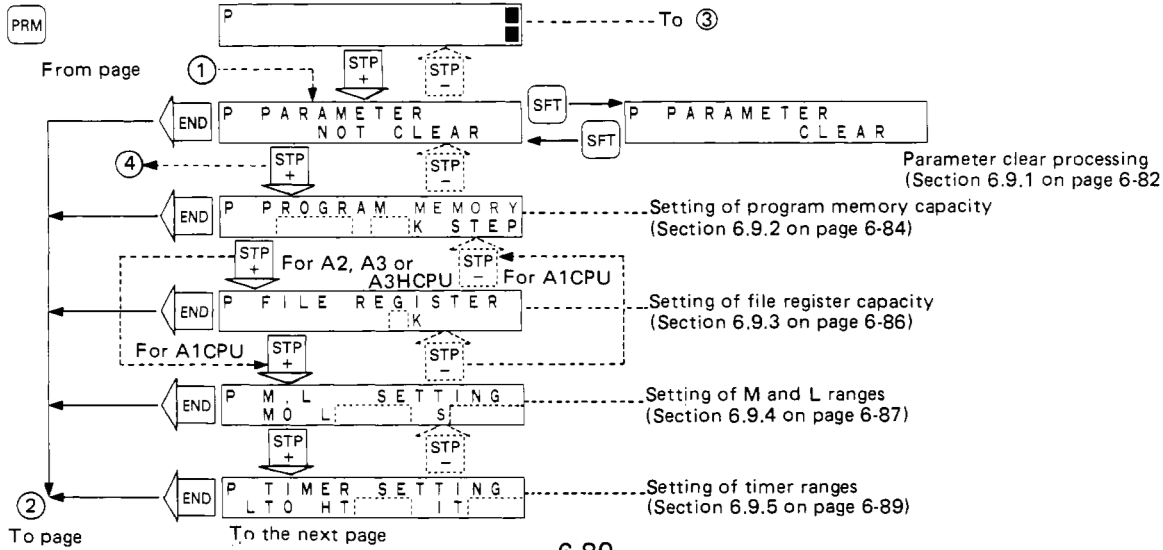
REMARKS

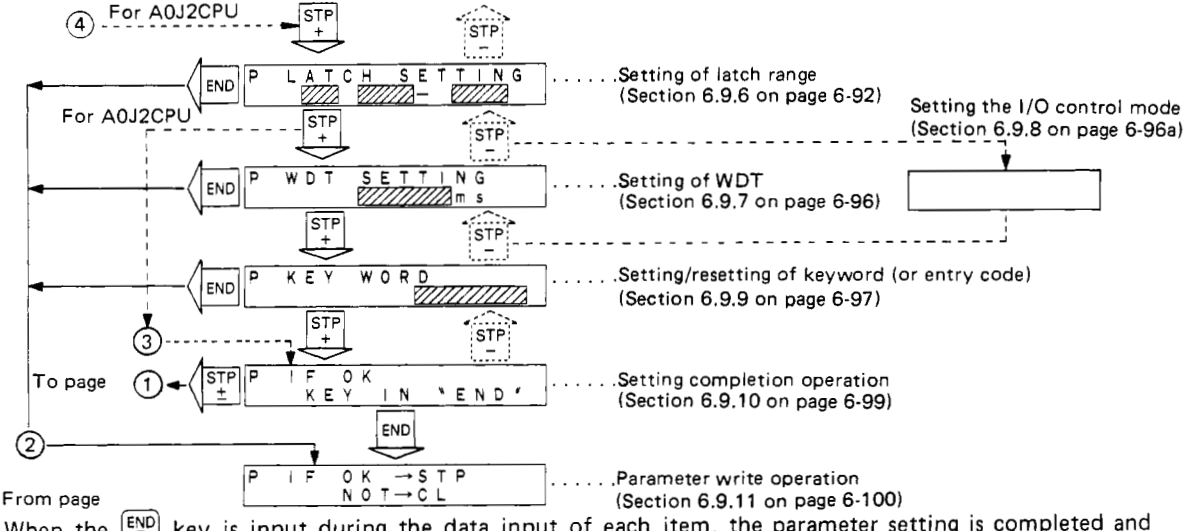
(1) The A7PU only allows the step relay (S) range to be read. The A6GPP/A6HGP/A6PHP must be used to set and change the step relay (S) range.

(2) The step relay (S) range is "S1536 to 2047" independently of the latch setting when step relay (S) "present" is set to the A0J2CPU.

(3) The step relay (S) has the same functions as the internal relay (M) and can be used in the same way as the internal relay (M) in the program.

Set parameters in the order that they are presented on the display, for each operation see sections 6.9.1 to 6.9.11.





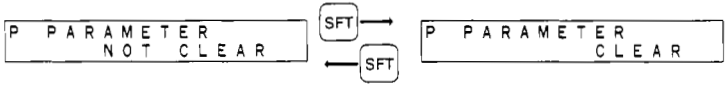
When the [END Z] key is input during the data input of each item, the parameter setting is completed and execution proceeds to Section 6.9.11 on page 6-100.

6.9.1 Clearing of parameters

Basic Operation

[SFT] ····· [SFT] → [STP +]

(1) Select display screen by pressing [SFT].



(2) When not clearing parameters

If the parameters set in the CPU are OK, select the screen shown below and press [STP +] or [STP −].

By the [STP +] input, the execution proceeds to the setting of program memory capacity (Section 6.9.2 on page 6-84). For the A0J2CPU, the execution proceeds to the setting of latch range (Section 6.9.6 on page 6-92).

By the [STP −] input, the execution proceeds to the setting completion operation (Section 6.9.10 on page 6-99).

(3) When clearing parameters

To change the parameters set in the CPU into default values, select the screen shown below and press STP +

```
P  PARAMETER
          CLEAR
```

By the STP + input, all the parameters are changed to default values and execution proceeds to the setting completion operation (Section 6.9.10 on page 6-99).

POINT

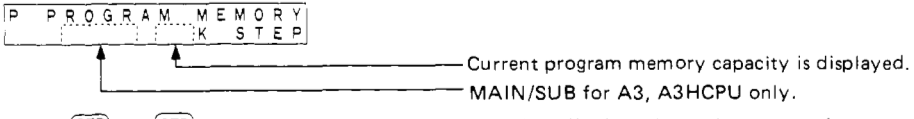
If a keyword (entry code) has been set, parameters cannot be cleared. Therefore, it is necessary to redefine the keyword (Section 6.9.9 on page 6-97).

6.9.2 Setting of program memory capacity (Other than A0J2CPU)

Basic Operation

- For A1 or A2CPU: Sequence program capacity → STP (+)
- For A3CPU or A3HCPU: Main sequence program capacity → STP (±) → Sub sequence program capacity → STP (±)
- When not changing the capacity: STP (±)

(1) For the setting of program memory capacity, the following screen is displayed.

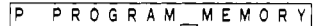


(2) By pressing STP (±) or STP (+), the program memory capacity displayed on the screen is entered as a parameter. (The setting unit is 1K step.)

(3) When the A3, A3HCPU is used, set the memory capacities of both the main program and subprogram. (When the subprogram is not required, set the subsequence program capacity of 0K step.)

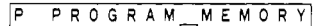
Operation example

For A1 or A2CPU



. . . . . .Present setting displayed.

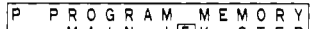
ORB 6



STP +

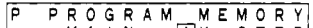
. . . .Program memory capacity is set to 6K steps. When the A1CPU is used, the execution proceeds to the setting of M and L ranges (Section 6.9.4 on page 6-87). When the A2CPU or A3CPU is used, execution proceeds to the setting of file register capacity (Section 6.9.3 on page 6-86).

For A3 or A3HCPU

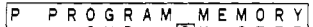


. . . . . .Present setting displayed.

SET 4

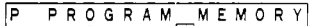


STP +



. . . . . .Press STP + to set main program capacity to 4K steps. Display shows present sub-program setting.

SET 4



STP +

. . . . . .Subprogram memory capacity is set to 4K steps and execution proceeds to the setting of file register capacity (Section 6.9.3 on page 6-86).

6.9.3 Setting of file register capacity (Other than A0J2 and A1CPU)

Basic Operation

- When changing: File register capacity → STP +
- When not changing: STP ±

(1) Set the file register capacity of A2, A3 or A3HCPU.
(The setting unit is 1K point. If the file register is not required, set the capacity to 0K point.)

Operation example

```
P FILE REGISTER
      3K
```
..... Present setting displayed.

SET 4

```
P FILE REGISTER
      4K
```

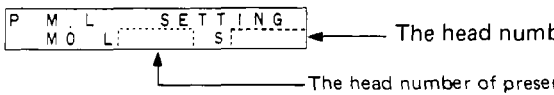
STP + ... File register capacity is set to 4K points and the execution proceeds to the setting of M and L ranges (Section 6.9.4 on page 6-87).

6.9.4 Setting of M and L ranges (Other than A0J2CPU)

Basic Operation

- When changing: Head number of L → STP ±
- When not changing: STP ±

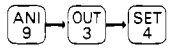
(1) For the setting of M and L ranges, the following screen is displayed.


P M . L SETTING
M 0 L S
The head number of presently set step relay (S) is displayed.
The head number of presently set latch relay (L) is displayed.

(2) Input the head number as described below:
The head number of L must not be greater than that of S and must not be less than that of M.
When M is not required, input "head number of L = 0."
When L is not required, input "head number of L = head number of S."

(3) By the input of STP ±, the head numbers are set to the numeric values displayed on the screen.

Operation example




```
P  M , L      S E T T I N G
   M 0   L 1 0 0 0 S 2 0 0 0
P  M , L      S E T T I N G
   M 0   L   9 3 4 S 2 0 0 0
```

..... Present setting displayed { M = 0 to 999 / L = 1000 to 1999 / S = 2000 to 2047

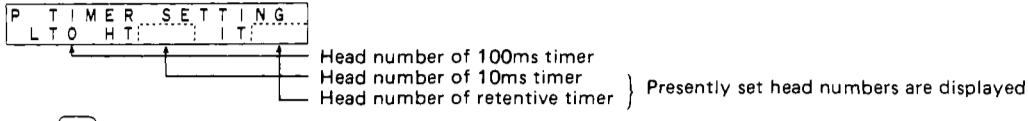
STP (+) ..... M is defined as 0 to 933 and L is defined as 934 to 1999 and S is defined as 2000 to 2047 the setting of timer range (Section 6.9.5 on page 6-89).

6.9.5 Setting of timer ranges (Other than A0J2CPU)

Basic Operation

- When changing: Head number of 10ms timer → SFT → Head number of retentive timer → STP ±
- When not changing: STP ±

(1) For the setting of timer ranges, the following screen is displayed.


P TIMER SETTING
LTO HT IT
Head number of 100ms timer
Head number of 10ms timer
Head number of retentive timer
Presently set head numbers are displayed.

(2) Press SFT to switch between the 10ms timer and the retentive timer.

(3) Input the head numbers as described below:
Head number of 100ms timer $\leqq$ head number of 10ms timer $\leqq$ head number of retentive timer
When the 100ms timer is not required, set the head number of the 10ms timer = 0.

When the 10ms timer is not required, set the head number of 10ms timer = head number of retentive timer.
When the retentive timer is not required, set the head number of retentive timer = 256.

Example: When not changing the range of 10ms timer but changing only the range of retentive timer, input [SFT], [Head number of retentive timer], and [STP ±].

(4) By the input of [STP ±], the head numbers are set to the numeric values displayed on the screen.
(5) Minimum setting in units of 8 timers. Be sure to set the head number of each timer so that it can be divided by 8.

Operation example

```
P  T I M E R   S E T T I N G
  L T 0   H T 2 0 0   I T 2 5 6
```

.....Present setting displayed

- 100ms (Low-speed) timer (LT) = 0 to 199
- 10ms (High-speed) timer (HT) = 200 to 255
- Retentive (Integrating) timer (IT) = No setting

SFT(1) → CJ(2) → LDI(8)

```
P  T I M E R   S E T T I N G
  L T 0   H T 1 2 8   I T 2 5 6
```

SFT

```
P  T I M E R   S E T T I N G
  L T 0   H T 1 2 8   I T 2 5 6
```

.....By SFT input, the cursor moves to the integrating timer side.

CJ(2) → RST(0) → RST(0)

```
P  T I M E R   S E T T I N G
  L T 0   H T 1 2 8   I T 2 0 0
```

STP(+).....The contents of screen display are set and the execution proceeds to the setting of latch range (Section 6.9.6 on page 6-92).

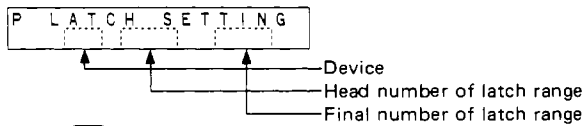
- 100ms (Low-speed) timer (LT) = 0 to 127
- 10ms (High-speed) timer (HT) = 128 to 199
- Retentive (Integrating) timer (IT) = 200 to 255

6.9.6 Setting of latch range (Other than A0J2CPU)

Basic Operation

- Latch range specification: Head number → SFT → Final number → STP ±
- When not executing latch: ' SP → STP ±

(1) For the setting of latch ranges, the following screen is displayed.



Devices are displayed by the following symbols:
- B = link relay
- LT = low-speed timer (100ms)
- HT = high-speed timer (10ms)
- IT = integrating timer (Retentive)
- C = counter
- D = data register
- W = link register

(2) Press SFT to switch between the head number and the final number of the latch range.

(3) Input the data as described below:

Head number of latch range ≦ the final number

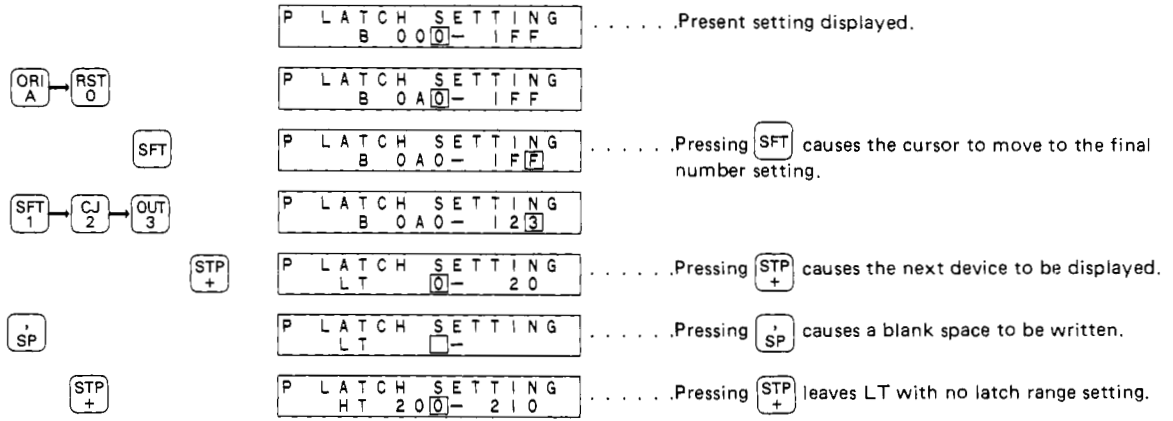
If the valves are to remain unchanged simply proceed to the next key stroke.

Use the ' SP key to input a blank spece where no latch range is required.

(4) By pressing [STP +], the following devices are displayed:
Device display order: B ⇄ LT ⇄ HT ⇄ IT ⇄ C ⇄ D ⇄ W (→ indicates [STP +] input and ← indicates [STP −] input.)
When [STP −] is pressed during the display of device B, execution returns to Section 6.9.5.
When [STP +] is pressed during the display of device W, execution proceeds to Section 6.9.7.

When the A3HCPU is used, execution proceeds to Section 6.9.8.

Operation example

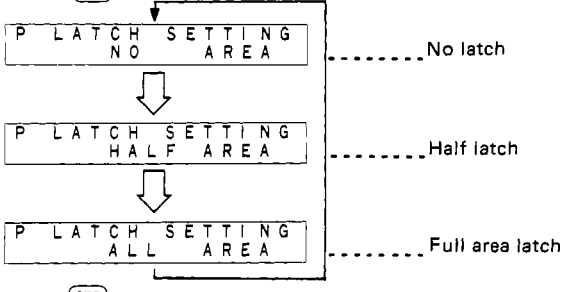

P LATCH SETTING
B 000- IFF
. . . . . Present setting displayed.
ORI A → RST 0
P LATCH SETTING
B 0A0- IFF
SFT
P LATCH SETTING
B 0A0- IFF
. . . . . Pressing SFT causes the cursor to move to the final number setting.
SFT 1 → CJ 2 → OUT 3
P LATCH SETTING
B 0A0- 123
STP +
P LATCH SETTING
LT 0- 20
. . . . . Pressing STP + causes the next device to be displayed.
, SP
P LATCH SETTING
LT -
. . . . . Pressing , SP causes a blank space to be written.
STP +
P LATCH SETTING
HT 200- 210
. . . . . Pressing STP + leaves LT with no latch range setting.

(A0J2CPU)

Basic Operation

SFT ····· SFT → STP (±)

(1) By the input of SFT key, select the display screen.



(2) By the input of STP (±), the displayed latch range is set.
By the input of STP (+), the execution proceeds to Section 6.9.9 (page 6-99).
By the input of STP (−), the execution proceeds to Section 6.9.2 (page 6-84).

6.9.7 Setting of WDT (Other than A0J2, A3HCPU)

Basic Operation

Watch dog timer value → STP ±

(1) By pressing STP ±, the numeric value displayed on the screen is set.

(2) The set value of WDT is in units of 10msec. The deast significant digit must be "0".

Operation example

```
P WDT SETTING
      100ms
```
. . . . . .Present setting displayed.

CJ 2 → RST 0 → RST 0

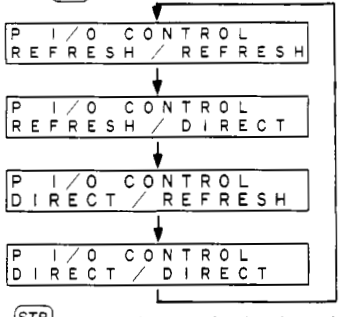
```
P WDT SETTING
      200ms
```

STP + ...The screen contents are set and execution proceeds to the setting/resetting of keyword (entry code) (Section 6.9.9 on page 6-97).

6.9.8 Setting the I/O control mode (A3HCPU)

Basic Operation

(1) Press the SFT key to select the required display screen.



. . . . . .Input and output in refresh mode

. . . . . .Input in refresh mode, output in direct mode

. . . . . .Input in direct mode, output in refresh mode

. . . . . .Input and output in direct mode

(2) Press STP ± to set the mode displayed on the screen.
Pressing STP + proceeds to Section 6.9.8.
Pressing STP − proceeds to Section 6.9.6.

6.9.9 Setting/resetting of keyword (entry code) (Other than A0J2CPU)

Basic Operation

- Setting of keyword (entry code) [KEY-WORD] → [STP ±]
- Resetting of keyword (entry code) [' SP] → [STP ±]

(1) Set or reset the keyword. (entry code)

(2) The keyword is made up of six hexadecimal digits.

Operation example

- When keyword has not been set

```
P KEY WORD □
```

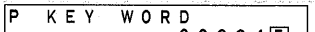
Since a keyword has not been set, display is provided in blank.

[SFT 1] → [CJ 2] → [OUT 3] → [SET 4]

```
P KEY WORD
          001234
```

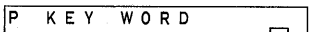
[STP ±] . . . . . Setting is complete for keyword and execution proceeds to the completion of settings operation (Section 6.9.10 on page 6-99).

• When keyword has been set



. . . . . .The keyword is displayed.

(, SP)



. . . . . .By (, SP) input, the keyword display is erased.

(STP +) . . . . . .Keyword resetting is complete and execution proceeds to the completion of setting operation (Section 6.9.10 on page 6-99)

• When changing the keyword (entry code):

1) Reset the keyword by the above operation.
2) Set a new keyword by the operation described on the preceding page.

6.9.10 Completion of setting operation

Basic Operation

- When parameter setting is completed and is to be loaded to the CPU [END]
- When changing the parameters [STP ±]

(1) The setting completion operation loads the parameters to the CPU or allows the parameters to be checked.

Operation example

```
P I F  0 K
    K E Y   I N   " E N D "
```

[END Z] . . . . . .The parameter setting is complete and the execution proceeds to the parameter write operation (Section 6.9.11 on page 6-100).

```
P I F  0 K
    K E Y   I N   " E N D "
```

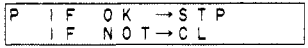
[STP ±] . . . . . .To check the parameters written, execution proceeds to the parameter clear operation (Section 6.9.2 on page 6-84) by the [STP +] input and proceeds to the setting/resetting of keyword (Section 6.9.9 on page 6-97) by the [STP −] input.

For the A0J2CPU, the execution proceeds to the setting of latch range (Section 6.9.6 on page 6-92).

6.9.11 Write of parameters

Basic Operation

- When writing parameters to the CPU [STP ±]
- When not writing parameters to the CPU [CL]



Press [STP ±] to load new parameters into the CPU.

Press [CL] to prevent loading and then press the [STP ±] key to change the relevant parameters by stepping through the parameters listed in Section 6.9.1 to 6.9.11.

Press (STP ±) to load parameters to CPU:

```
P  RUN(PARAMETER)
     3          ***
```

.....During write to the CPU, * marks are displayed.
(One * mark indicates 1K byte.)

Indicates the total number of bytes.

```
P  RUN(PARAMETER)
   COMPLETION
```

.....Displayed on completion.

When selecting the audio cassette function, reset as described in Section 5.6 on page 5-16.

7. AUDIO CASSETTE INTERFACE OPERATION PROCEDURES

The audio cassette function allows the record (write), replay (read), and verify of data shown in Table 7.1. The record (write) and verify operations can be performed during CPU run. The replay (read) operation can be performed only during CPU stop.

Data name \ CPU Type	A1CPU	A2CPU	A3CPU	A3HCPU
Parameter	○	○	○	○
Program	○	○	○	○
Parameter + program	○	○	○	○
Subprogram	–	–	○	○
Device memory	○	○	○	○
File register	–	○	○	○
Comment	○	○	○	○
Status latch	–	○	○	○
Sampling trace	–	○	○	○
Memory cassette	–	○	○	○
Others (General data)	○	○	○	○

Table 7.1 Data Processed by Audio Cassette Function (○ = allowed)

7.1 Operation Instructions

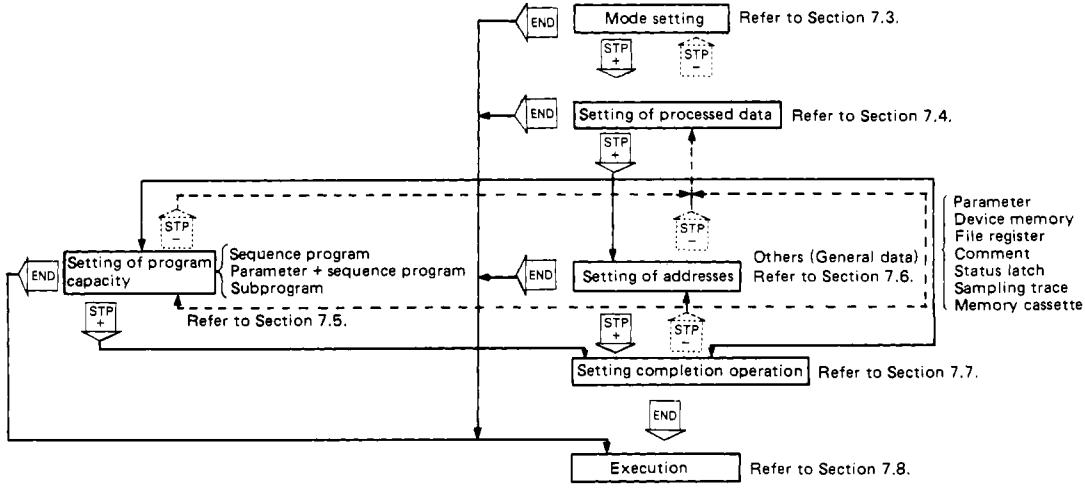
(1) For the read or verify operation, set the volume of the audio cassette to maximum. (Refer to Appendix 1.)
(2) For the selection of tape recording time, refer to the list of processing times in the Appendix.
(3) Normal domestic cassettes may be used-however those sold for home computer use are recommended.
(4) A tape recorded with the A6PU can be replayed to the CPU via the A7PU.
(5) If device memory data recorded from the A0J2CPUP23/R23 is replayed to the A0J2CPU, verify error will occur. If device memory data recorded from the A0J2CPU is replayed to the A0J2CPUP23/R23, link register contents will be lost.

POINT

See Appendix 2 for required processing times. For memory capacities > 64K the A6GPP programs should be stored on floppy disk due to the long time required with the PU.

7.2 General Operation for Audio Cassette Function

The general operation for the audio cassette function is explained below.



7.3 Mode Setting

Basic Operation

(SFT ···) STP ±

Mode selection

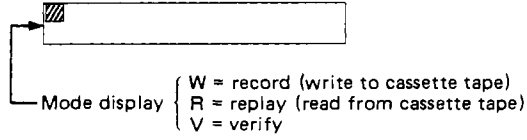
(1) By pressing the SFT key, switch the display screen. (Mode selection)

(2) By pressing STP ±, the mode displayed on the screen is set.

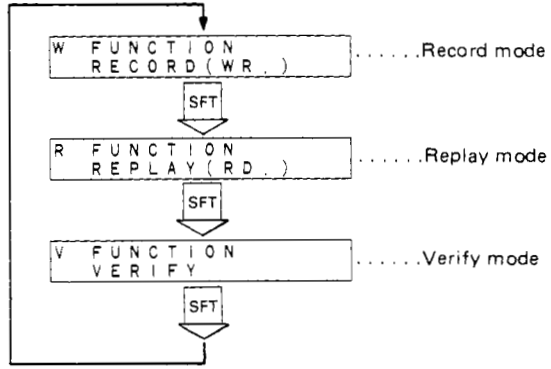
STP + ... Execution proceeds to Section 7.4.

STP − . . . . . Execution proceeds to Section 7.7.

The mode selection result is shown at the left top of screen.



Operation example



7.4 Setting of Processed Data

Basic Operation (SFT ···) STP ±

Processed data selection

(1) By pressing the SFT key, switch the display screen. (Selection of processed data)

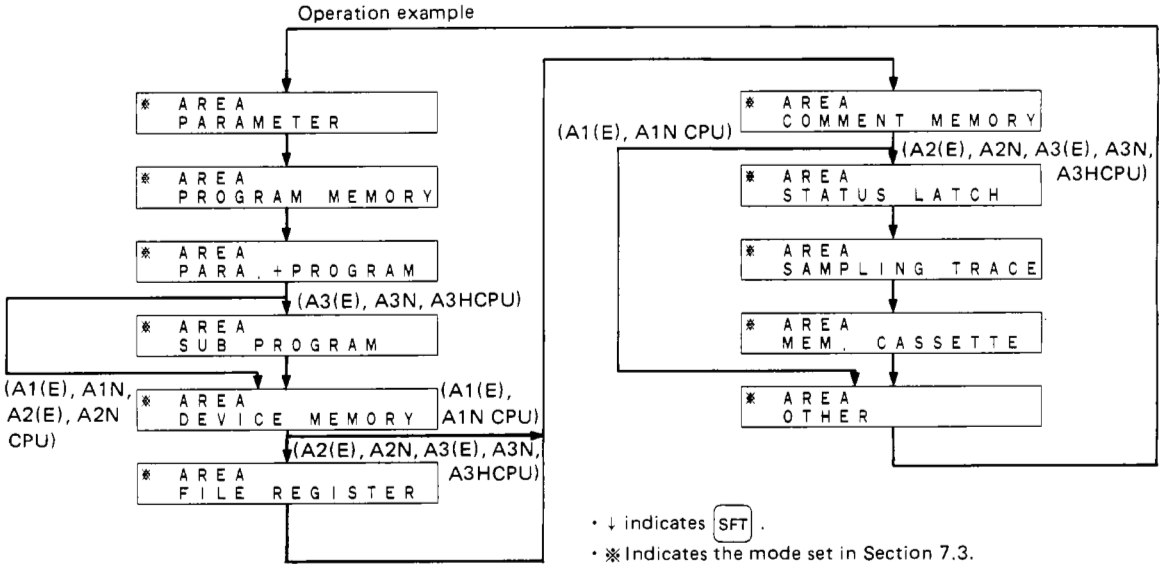
(2) By the input of STP ±, the mode displayed on the screen is set.

STP + ... Execution proceeds to Section 7.5, Section 7.6, or Section 7.7 depending on the selected data.

- Parameter (Other than A0J2CPU) . . . . . To Section 7.7
- Program, Parameter + program (Other than A0J2CPU), Subprogram (only A3(E), A3N, A3HCPU) . . . . . To Section 7.5
- Device memory (except X, Y, special M, special D), File register (A2(E), A2N, A3(E), A3N, A3HCPU), Comment, Status latch (A2(E), A2N, A3(E), A3N, A3HCPU), Sampling trace (A2(E), A2N, A3(E), A3N, A3HCPU), Memory cassette (only RAM area of A2(E), A2N, A3(E), A3N, A3HCPU) . . . . . To Section 7.7
- Others (General data) . . . . . To Section 7.6

STP − . . . . . Execution returns to Section 7.3.

(3) This operation is required for all, record, replay, and verify modes.



- ↓ indicates (SFT).
- ※ Indicates the mode set in Section 7.3.

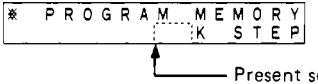
7.5 Setting of Program Capacity

Basic Operation

Sequence program capacity → STP (±)

(1) Setting of program capacity is required when the following data has been set by the operation described in Section 7.4.
- Program
- Parameter + program
- Subprogram (A3(E), A3N, A3HCPU)

(2) For the setting of program capacity, the following screen is displayed.



※ Indicates the mode.

Present setting displayed.

(3) By the input of STP (±), the numeric value displayed on the screen is set.

STP (+) . . . . . .Execution proceeds to Section 7.7.

STP (−) . . . . . .Execution returns to Section 7.4.

(4) When it is necessary to record a sequence program and a microcomputer program together, set the program capacity to include the microcomputer program capacity.

Example: When the sequence program capacity is 6K steps and the microcomputer program capacity is 4K bytes,

$$6\text{K steps} + \frac{4\text{K bytes}}{2\text{ bytes/steps}} = 6 + 2 = 8\text{K steps}$$

Operation example

```
* PROGRAM MEMORY
        4K STEP
```
. . . . . .Present setting displayed

```
* PROGRAM MEMORY
       12K STEP
```

SFT (1) → CJ (2)

STP (±) . . . . . .12K steps are to be processed.

※ Indicates the mode set in Section 7.3.

REMARKS

When program is selected for the A0J2CPU, record, replay or verify is enabled for parameter + program.

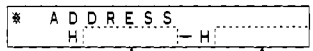
7.6 Setting of Addresses

Basic Operation

Head address → SFT → Final address → STP ±

(1) The address setting operation is required when the following data has been set by the operation described in Section 7.4.
- Other (General data)

(2) For the setting of address, the following screen is displayed.



※ Indicates the mode.

Head address
Final address
} Present setting displayed (5 digit hexadecimal.)

(3) By pressing SFT, the cursor moves between the head address and the final address.

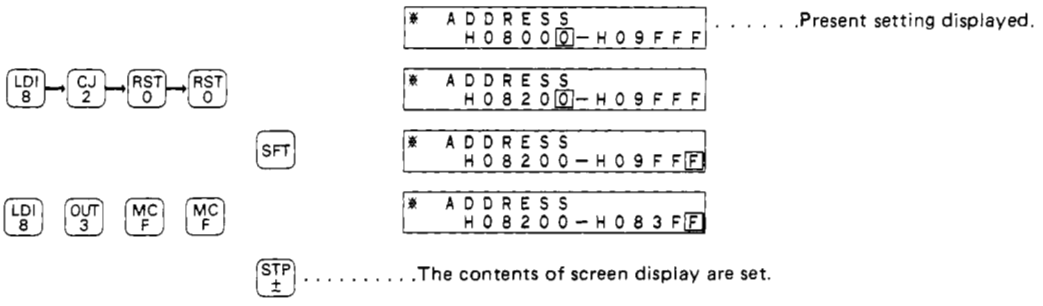
(4) If the address is not to be changed, input can be omitted.

(5) By pressing STP ±, the numeric value displayed on the screen is set.

STP + ...Execution proceeds to Section 7.7.

STP − . . . . . .Execution returns to Section 7.4.

Operation example



※ Indicates the mode set in Section 7.3.

7.7 Setting Completion Operation

Basic Operation

- When making no change after completing the setting [END]
- When making any changes. [STP ±]

(1) The setting completion operation is used to complete or change (check) data settings.

Operation example

```
* IF OK
  KEY IN 'END'
```

[END Z] . . . . Completes setting and proceeds to execution operation (Section 7.8).

```
* IF OK
  KEY IN 'END'
```

[STP ±] . . . . To change or check data settings. Screen returns to mode setting (Section 7.3 on page 7-4).

By pressing [STP −], execution returns to the operation (Section 7.4 Section 7.5 or Section 7.6) immediately prior to the setting completion operation.

7.8 Execution Operation

Basic Operation
- When executing processing [STP ±]
- When not executing processing [CL]

(1) The execution operation is used to execute or not to execute the mode set in Section 7.3.

Operation example

```
* IF OK →STP
  IF NOT→CL
```

※ Indicates the mode.

[STP ±] . . . . . .Executes the mode set. Start cassette recorder before pressing [STP ±] .

To stop processing during execution, press the [CL] key.
When the [CL] key is pressed, the following message is displayed.

```
* RUN [      ]
  STOP
```

(RECORD), (REPLAY), or (VERIFY) is displayed in [ ] .

Upon completion of execution, the following screen is displayed. By pressing [STP ±] after completion, execution returns to Section 7.3.

```
* RUN
  COMPLETION
```

[CL] . . . . . .Allows re-setting (Section 7.3 to 7.7)

Record operation example

```
W IF OK →STP
  IF NOT→CL
```

[STP ±]

```
W RUN(RECORD)
  20 **********
```

During execution, the RUN display flickers and the remaining amount of memory displayed at the bottom of screen.

One * mark indicates 1K byte.

POINT

Note the approximate processing time in the Appendix before selecting the audio cassette tape to be used.

Replay and verify operation example

```
* IF OK →STP
  IF NOT→CL
```

The ※ R displayed during replay and V displayed during verify.

[STP ±] ------ Executes level matching check. If OK, the following display is provided.

```
* RUN
  LEVEL OK
```

In side [------] , (REPLAY) or (VERIFY) is displayed as appropriate.

```
* RUN
  28 ********
```

.....During execution, the RUN display flickers and the remaining amount of memory is displayed at the bottom of the screen.

If the level matching check result is not satisfactory, the following screen is displayed for approximately 60 seconds.
In this case the volume of the audio cassette. When the level is OK, the screen shown above is displayed.

```
* RUN
  LEVEL NG
```

If the level does not become OK during the level check (Which lasts approximately 60 seconds), "LEVEL ERROR" is displayed. In this case, press [STP ±], rewind the tape, and repeat the operation.

8. ERROR MESSAGE LIST

This chapter describes error messages and corrective actions during programming and use of cassette interface.

8.1 Error Messages for Programming Function

If an error message is displayed, press the relevant mode key and repeat the operation correctly.

No.	Display	Display Condition	Corrective Action
1	A C P U R U N	Write, insert/delete mode, or another mode has been attempted during CPU run.	Set to CPU stop.
2	C A N T F I N D	Data has been searched but cannot be found.	———

No.	Display	Display Condition	Corrective Action
3	CANT OPERATE	The correct keyword has not been entered	Restart the PU and key-in the correct entry code.
4	CODE ERROR	The instruction code has been corrupted or semi-deleted.	When the CPU has detected an error, set the CPU from RUN to STOP status, reset the CPU, then check instructions located in front of and behind the step where the error has occurred, and write correct instruction.
5	DEVICE ERROR	The set device symbol is wrong. The device number is outside the range specified.	Re-set.
6	DUAL COIL ERROR	The coil already exists in the program.	If the program is correct, leave it as it is. Otherwise change the coil designation.
7	INS SET ERROR	The instruction set in the read, write, or insert mode is not correct.	Re-set.

No.	Display	Display Condition	Corrective Action
8	MODE SET ERROR	Mode selection has not been made.	Select mode.
9	OPERATION ERROR	An operation mistake has been made.	Check key operation.
10	PARAMETER ERROR	The assignment of memory set by parameters has exceeded the capacity of memory cassette.	Correct the memory assignment.
11	PC NOT RESPOND	Communication cannot be made with the CPU.	Perform operation again. If communication cannot be made, check the following: { PU { Cable connection condition { CPU
12	PC WRITE ERROR	Data could not be written to the CPU.	Check the setting of RAM/ROM. Check the loading of RAM, etc. Check the memory protect switch of CPU.
13	SETTING ERROR	Non valid parameter setting.	Check correct setting.

No.	Display	Display Condition	Corrective Action
14	STEP OVER ERROR	The set step number is greater than the largest step number.	Set correct step number.
15	WR ADDR ERROR	Write-in access has been attempted to a write-forbidden area.	Set correct address.
16	MEMORY PROTECT	During write in write, insert, delete mode, etc., memory protect switch of the memory cassette is ON.	Set memory protect switch to OFF.
17	CASSETTE ERROR	During communication with the CPU in entry code clear, parameter write, or MT mode, memory cassette is faulty or is not loaded.	Load memory cassette. Change memory cassette.

8.2 Error Messages for Audio Cassette Function

No.	Display	Display Condition	Corrective Action
1	ACPU RUN	Replay has been attempted during CPU run.	Stop the CPU.
2	LEVEL ERROR	• The level does not match because of volume setting during replay or verify. (The level NG display is provided after a certain period of time (approximately 60 seconds).) • The audio cassette does not operate during replay or verify.	Re-set the volume of audio cassette to the optimum value. (Refer to Appendix 1.)
3	MT ERROR	• A sum check error has occurred with respect to the sum check code recorded on the tape. • Data in excess of the data recorded on the tape has been attempted to be replayed or verified.	Change the tape. Set correct setting range.
4	PARAMETER ERROR	The assignment of memory set by parameters replayed from the tape, has exceeded the capacity of the memory cassette.	Load correct memory cassette or check the combination of memory cassette and tape.

No.	Display	Display Condition	Corrective Action
5	PC NOT RESPOND	Proper communication cannot be made with the CPU.	Check cable connection, etc.
6	SETTING ERROR	The set value is not correct.	Perform correct setting.
7	VERIFY ERROR	A verify error has occurred. Device memory data recorded from the A0J2CPUP23/R23 has been re-played to the A0J2CPU.	———

8.3 Error Number and Error Message List

When an error has occurred in the programmable controller CPU, one of the following messages is displayed by the operation described in Section 6.8.5 on page 6-69(TEST → K → STP ±).

ERROR No.	Error Message	Description	Corrective Action
10	INS. CODE ERROR	An instruction code, which cannot be decoded by the CPU, is included in the program. 1) A ROM including an instruction code, which cannot be decoded, has been loaded. 2) The contents of memory have changed for some reason and an instruction code, which cannot be decoded, has been included.	Read the error step and correct the instruction at that step. When the cause of trouble is the ROM, rewrite the contents or change it.
11	PARAMETER ERROR	1) A capacity larger than the memory capacity of CPU has been attempted to be written. 2) The parameter contents of CPU memory have changed due to noise or improper loading of memory.	1) Check the parameter contents and re-set them by the PU. 2) Check the loading of CPU memory.

ERROR No.	Error Message	Description	Corrective Action
12	M I S S I N G E N D I N S	The END instruction does not exist in the program.	Write END at the end of program.
13	C A N ' T E X E C U T E	1) There is no jump destination or there are several jump destinations specified for CJ, SCJ, CALL, CALLP, or JMP instruction. 2) There is a CHG instruction but there is no subprogram setting. 3) Although there is no CALL instruction, a RET instruction is in the program and has been executed. 4) The jump destination of CJ, SCJ, CALL, CALLP, or JMP instruction is located below the END instruction and has been executed.	Read the error step by the PU and correct the program at that step. (Insert jump destination or reduce the number of jump destinations to one.)

ERROR No.	Error Message	Description	Corrective Action
15	CAN'T EXECUTE	1) Although an interruption unit is used, the interruption pointer I, does not exist for that unit in the program or there are several occurences. 2) An IRET instruction is not included in the interruption program. 3) There is an IRET instruction other than in the interruption program.	1) Check if there is an interruption program, which corresponds to the interruption unit, or reduce the occurences of I to one. 2) Check if there is an IRET instruction in the interruption program. 3) Check if there is an IRET instruction in other than the interruption program and delete the IRET instruction.
16	CASSETTE ERROR	A memory cassette is not loaded.	Load a memory cassette and perform reset.
20	RAM ERROR	After checking if the CPU can perform write and/or read operation to and/or from the data memory area of CPU, either or both could not be performed.	The cause is a hardware error, consult the nearest sales representative.
21	OPE. CIRCUIT ERR	The operation circuit, which performs sequence processing inside the CPU, does not work properly.	

ERROR No.	Error Message	Description	Corrective Action
22	WDT ERROR	Scan time has exceeded the watch dog timer error supervising time. 1) The scan time of user program has exceeded the WDT valve due to program. 2) Instantaneous power failure has occurred during scan and the scan time has increased.	1) Calculate and check the scan time of user program and reduce the scan time by use of CJ instruction, etc. 2) Monitor the content of special register D9005. When it is other than 0, check the power and reduce voltage variations because the power voltage is unstable.
23	SUB-CPU ERROR	The sub-CPU has malfunctioned.	The cause is a hardware error, consult the nearest sales representative.
24	END NOT EXECUTE	1) When the END instruction is executed, another instruction code has been read due to noise, etc. 2) The END instruction has changed to another instruction code for some reason.	Perform reset and run the CPU again. If the same error is displayed again, the cause is a hardware error, consult the nearest sales representative.
26	WDT ERROR	The main CPU has executed an endless loop or has malfunctioned. (The sub-CPU makes check.)	The cause is a hardware error, consult the nearest sales representative.

ERROR No.	Error Message	Description	Corrective Action
31	UNIT VERIFY ERR	I/O unit data is different from that at power-on. 1) An I/O unit has been removed during operation or a different unit has been loaded. 2) The above has occured during stop and then the CPU has been set to RUN status.	1) Since the bit of special register D9116 to D9123, which corresponds to the unit where a verify error has occurred, is "1", monitor the special registers by the PU and check and change the relevant unit. 2) If the present unit arrangement is OK, perform reset by the RESET switch.
32	FUSE BREAK OFF	A fuse has blown in an output unit.	1) Check the fuse blow indicator LED of output unit. 2) Monitor special registers D9100 to D9107 and change the fuse of unit corresponding to the special register of which bit is "1".

ERROR No.	Error Message	Description	Corrective Action
40	CONTROL BUS ERR	The FROM and TO instructions cannot be executed. Control bus error with respect to a special unit.	The cause is a hardware error in special unit, CPU unit, or base unit, change the unit and consult the nearest sales representative.
41	SP.UNIT DOWN	When the FROM or TO instruction is executed, access has been made to a special function unit which has not responded. 1) The accessed special function unit is defective.	Since this is a hardware error of the special unit, consult the nearest sales representative.
42	LINK UNIT ERROR	1) AJ71R22 or AJ71P22 is loaded in the master station. 2) Two or more AJ71R22 or AJ71P22 are loaded in a local station.	1) Remove the AJ71R22 or AJ71P22 from the master station. 2) Only one AJ71 R22 or AJ71P22 should be loaded in the local station. After correction reset.

ERROR No.	Error Message	Description	Corrective Action
43	I/O INT. ERROR	Interruption has occured with out interrupt unit being loaded.	Hardware error. Consult the nearest sales representative.
44	SP. UNIT LAY ERR	1) Three or more computer link units are loaded on one CPU unit. 2) Two or more AJ71P22 or AJ71R22 are loaded. 3) Two or more interruption units are loaded.	1) Max. of two computer link units allowed. 2) Only one AJ71P22 or AJ71R22 allowed. 3) Only one interrupt unit allowed.
46	SP. UNIT ERROR	Access (execution of FROM or TO instruction) has been made to a location where there is no special function unit.	Check and correct the content of FROM or TO instruction.
47	LINK PARA ERROR	Link parameters are incorrect.	1) Write parameters again. 2) If parameters are correct but the message is still displayed, the cause is a hardware error. Therefore, consult the nearest sales representative.

ERROR No.	Error Message	Description	Corrective Action
50	OPERATION ERROR	1) The result of BCD conversion has exceeded the specified range (9999 or 99999999). 2) Setting has been performed exceeding the specified device range and operation cannot be performed.	Read the error step, check and correct the program at that step. (Check the device setting range, BCD conversion value, etc.)
70	An error code is displayed (no message)	1) The battery voltage has reduced. 2) The battery lead is disconnected.	1) Change the battery. 2) When RAM memory or power failure compensation is necessary, connect the battery.

APPENDICES

APPENDIX 1 Level Matching of Audio Cassette

This chapter describes the levels, classified by the models of audio cassettes. The following models has been checked as of May, 1986 and are examples only, this should not be taken as an indication of the models availability in a given country.

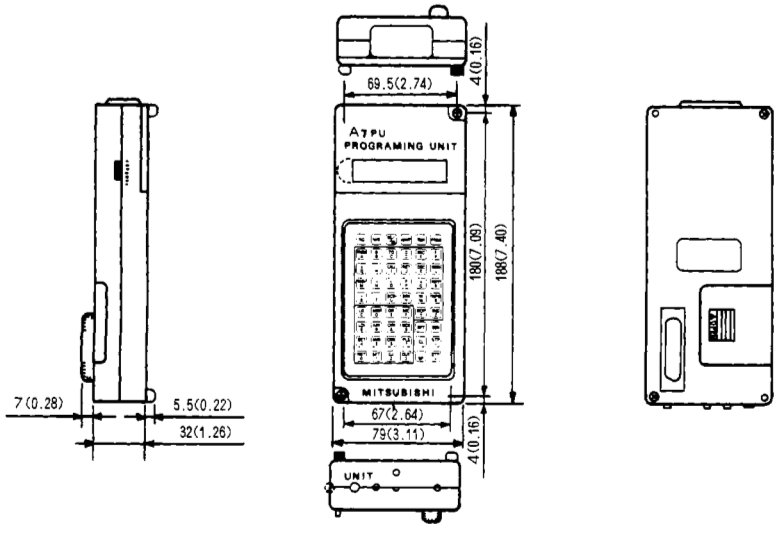
Audio Cassette Type	Volume Graduation during Replay or Verify	Remarks
CS-665 (by Fairmate)	0(min) 5 10(max)	Set the volume graduation to the range from 5/10 to 10/10.
RT-F33 (by Toshiba)	0(min) 5 10(max)	Set the volume graduation to the range from 4/10 to 10/10.
RQ-341 (by National)	0(min) 5 10(max)	Set the volume graduation to the range from 4/10 to 7.5/10.
RQ-2739 (by National)	0(min) 5 10(max)	Set the volume graduation to the range from 4.5/10 to 10/10.
RX-1835 (by National)	0(min) 5 10(max)	Set the volume graduation to the range from 2/10 to 10/10.
TC-1100 (by Sony)	0(min) 5 10(max)	Set the volume graduation to the range from 5.5/10 to 10/10.

APPENDIX 2 Processing Time for Audio Cassette Function

Data Name	Capacity	Processing Time	Remarks
Parameter	3K bytes	Approx. 2 min.	
Main program Subprogram	6K steps	Approx. 6 min.	
	14K steps	Approx. 12 min. 25 sec.	
	30K steps	Approx. 25 min. 10 sec.	
Device memory	6.5K bytes	Approx. 3 min. 25 sec.	
File register	8K bytes (4K points)	Approx. 4 min.	
Comment	64K bytes (4032 points)	Approx. 26 min. 25 sec.	
Status latch	28K bytes	Approx. 12 min.	
Sampling trace	8K bytes	Approx. 4 min.	

Data Name	Capacity	Processing Time	Remarks
Memory cassette	16K bytes (A3MCA-0)	Approx. 7 min. 15 sec.	
	16K bytes (A3MCA-2)	Approx. 7 min. 15 sec.	
	32K bytes (A3MCA-4)	Approx. 13 min. 35 sec.	
	64K bytes (A3MCA-8)	Approx. 26 min. 25 sec.	
	96K bytes (A3MCA-12)	Approx. 39 min. 50 sec.	
	144K bytes (A3MCA-18)	Approx. 58 min. 20 sec.	
Others (General data)	4K bytes	Approx. 2 min. 25 sec.	
	10K bytes	Approx. 4 min. 40 sec.	

APPENDIX 3 External Dimension Diagram



Unit: mm(inch)

IMPORTANT

The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(1) Ground human body and work bench.

(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your sp[redacted] application.

When exported from Japan, this manual does not require application to the Ministry of International Trade and Industry for service transaction permission.

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